Hybrid 7z24 Traveler

June 6, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens: HV+ with soldered wire.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7Z24 has die: 241-018 224-040 241-020 241-025 241-027 241-029 241-032

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7z24 classification info. Created 10:33:48 06/05/00

Hybrid 7z24 quality: fair
Chip classification: fair fair good fair fair fair fair
Bad channels (chip-channel): 0-91 1-103 3-83 4-24 5-53 6-56
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-11-82 3-20-82 3-21-82
   3-4-82 3-7-82 3-9-82 6-21-56 6-35-56 6-36-56 6-39-56 6-45-56
   6-6-56
Channels at pedestal needed for DCMS: 33.7 31.7 32.6 32.5 33.3 29.7 33.6
```

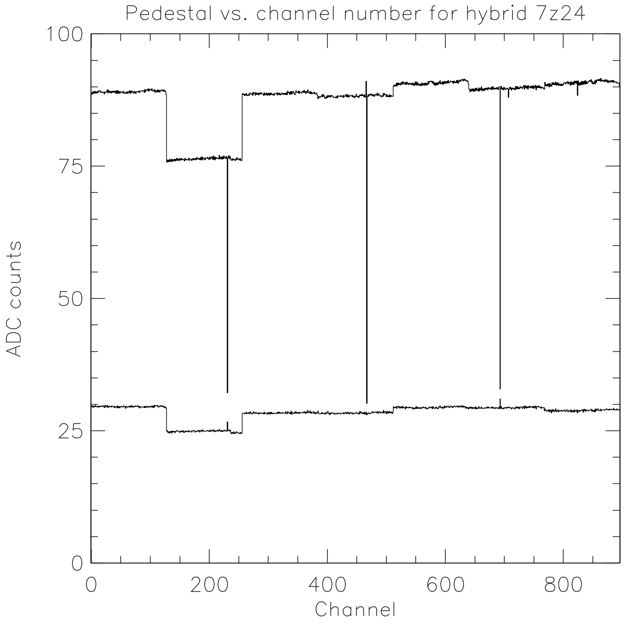
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

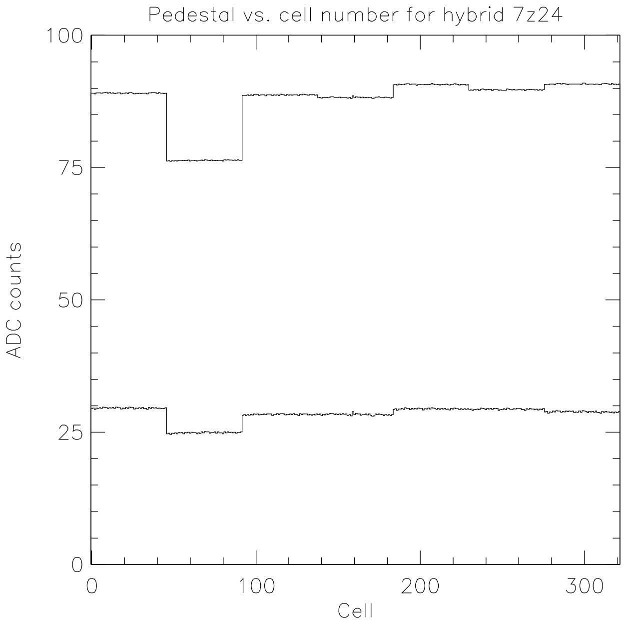
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

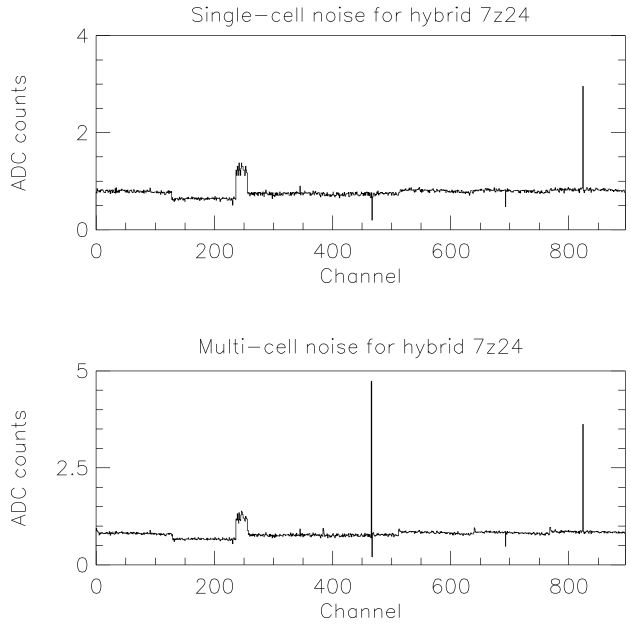
Pedestal vs. Pipeline Cell ID



6 Noise

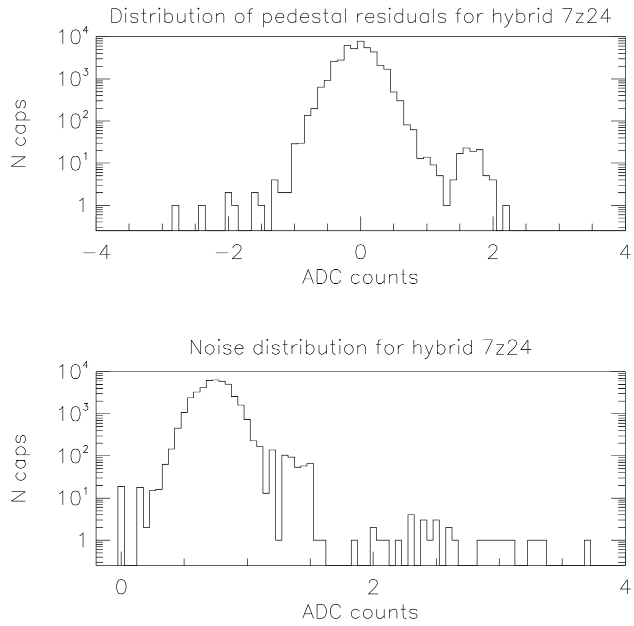
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in