Hybrid 7z3 Traveler

May 18, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7Z3 has die: 246-124 246-125 246-126 246-127 246-129 246-130 246-131

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7z3 classification info. Created 09:35:35 05/18/00

Hybrid 7z3 quality: fair
Chip classification: fair good good fair fair good fair
Bad channels (chip-channel): 0-13 0-80 3-114 6-70
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-18-108 0-18-109 0-19-108
   0-20-108 0-23-108 0-3-108 0-31-108 4-1-74 4-1-75 4-17-74 4-17-75
   4-18-74 4-2-74 4-27-74 4-30-74 4-4-74 4-4-75 4-43-74 4-43-75
   4-6-74 4-6-75 4-8-74 4-8-75
Channels at pedestal needed for DCMS: 35.5 32.7 31.7 31.6 33.6 33.6 32.1
```

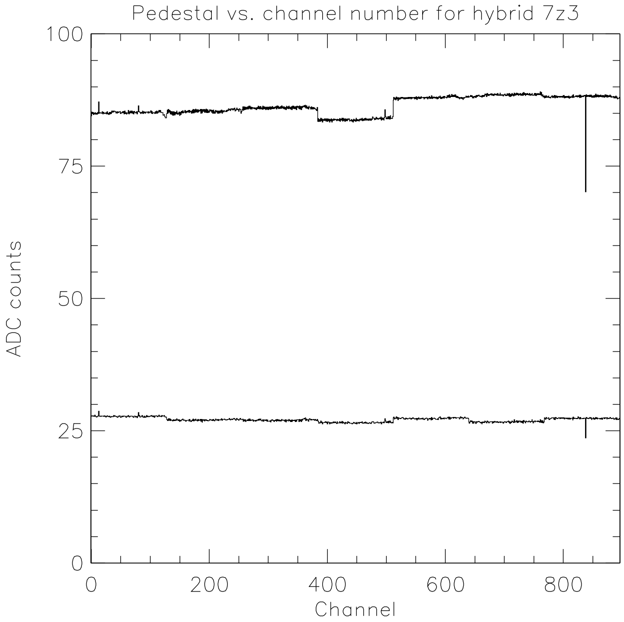
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

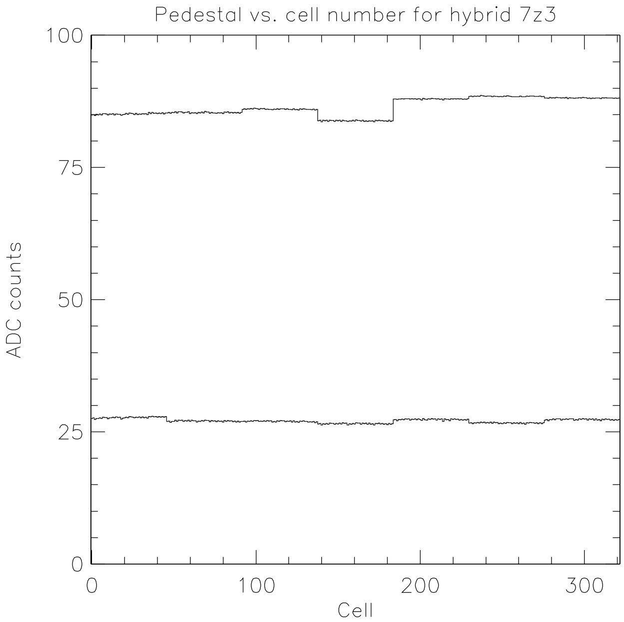
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

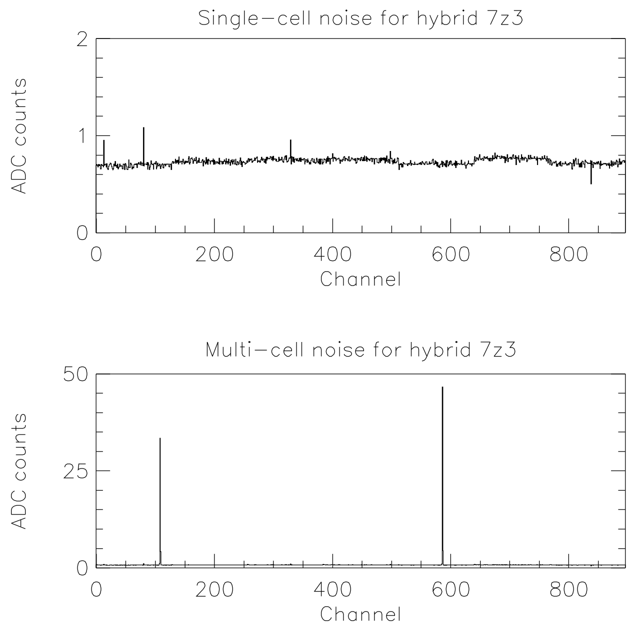
Pedestal vs. Pipeline Cell ID



6 Noise

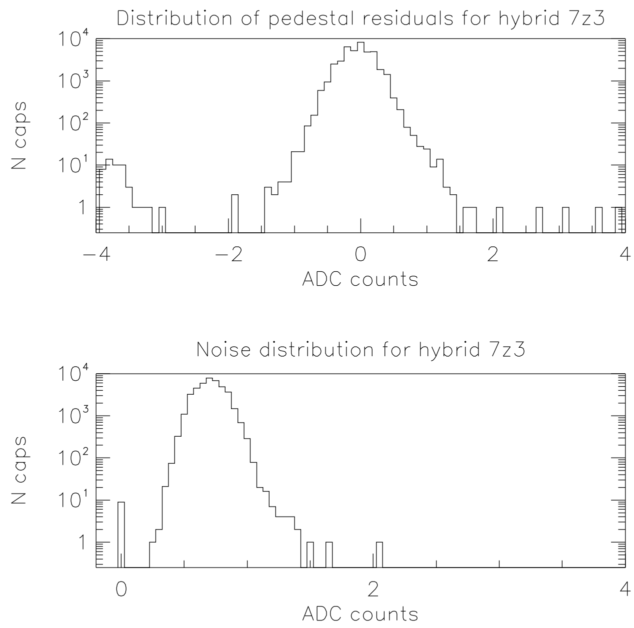
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in