Hybrid 7z86 Traveler

June 8, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 7Z86 has die: 229-046 229-049 229-051 229-053 229-062 229-073 229-077

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 7z86 classification info. Created 09:30:30 02/14/00

Hybrid 7z86 quality: fair*
Chip classification: fair* good good fair fair fair fair
Bad channels (chip-channel): 0-2 0-49 0-116 0-117 3-21 3-22 4-55 5-86 6-1 6-96
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-17-50 0-35-13 0-36-67
   3-17-95 4-32-12
Channels at pedestal needed for DCMS: 34.8 33.8 36.6 34.7 32.3 32.7 35.6
```

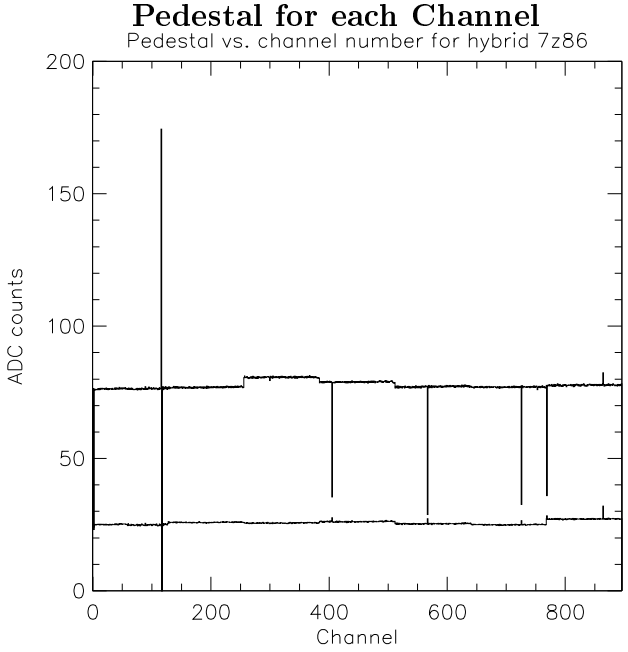
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

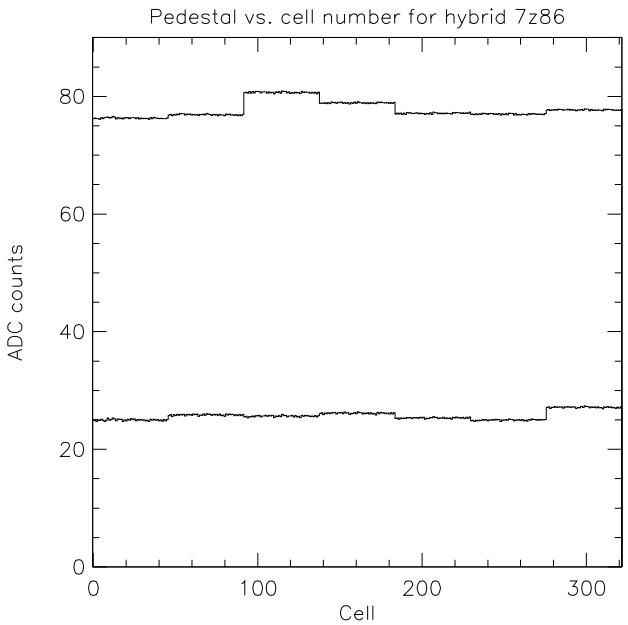
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

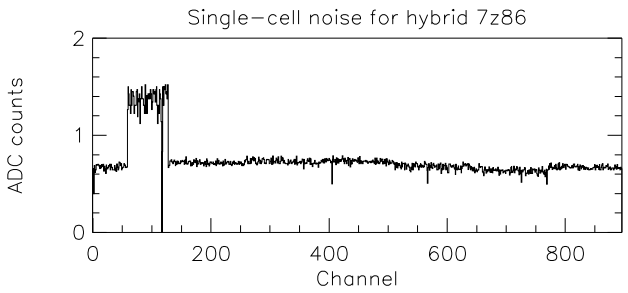
Pedestal vs. Pipeline Cell ID

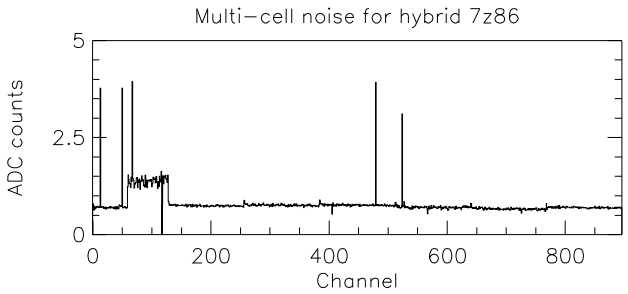


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

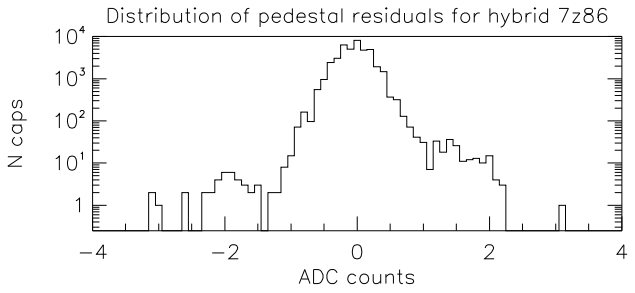
RMS Noise

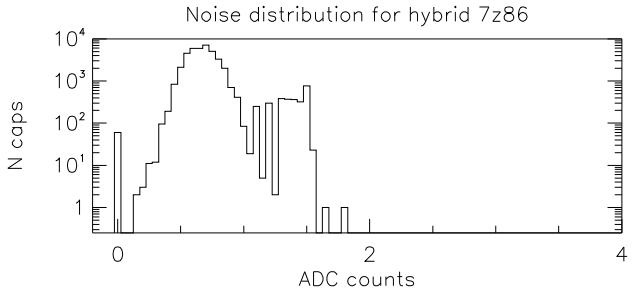




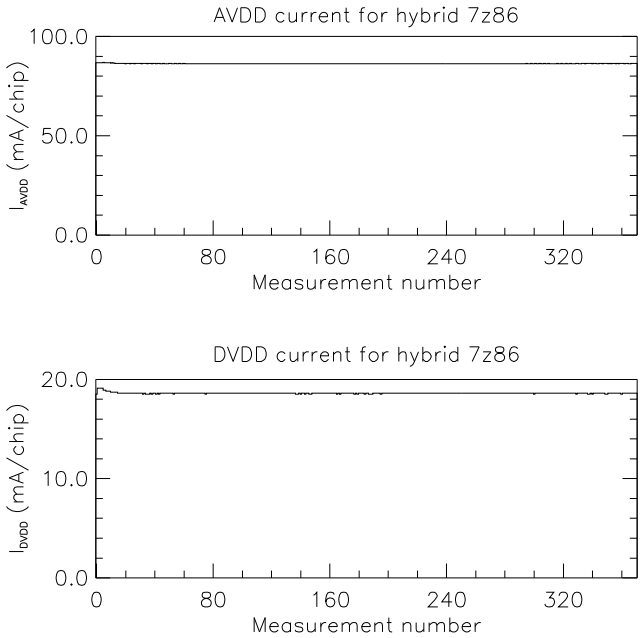
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in