Hybrid 8j1 Traveler

November 9, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J1 has die: 086-045 088-002 088-005 088-006 001-029 001-030 001-031 001-032

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid v3-001 classification info. Created 18:26:48 10/22/99

Hybrid v3-001 quality: bad
Chip classification: bad bad bad bad bad bad bad bad
Bad channels: N_bad_total = 1024 (too many to list all of them)
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-0-1 3-0-93 3-12-93 3-15-1 3-23-1 3-24-1 3-37-1 3-38-1 3-45-1 3-7-1 3-8-1 4-15-68 4-15-69 4-16-69 4-20-68 4-20-69 4-21-69 4-23-68 4-23-69 4-25-68 4-25-69 4-27-68 4-27-69 4-3-68 4-3-69 4-36-68 4-36-69 4-37-69 5-22-65 6-10-19 7-0-73 7-25-3 7-28-106 7-29-126 7-31-14 7-37-39
Channels at pedestal needed for DCMS: 36.6 34.4 35.6 34.6 35.6 36.3 35.6 34.7
```

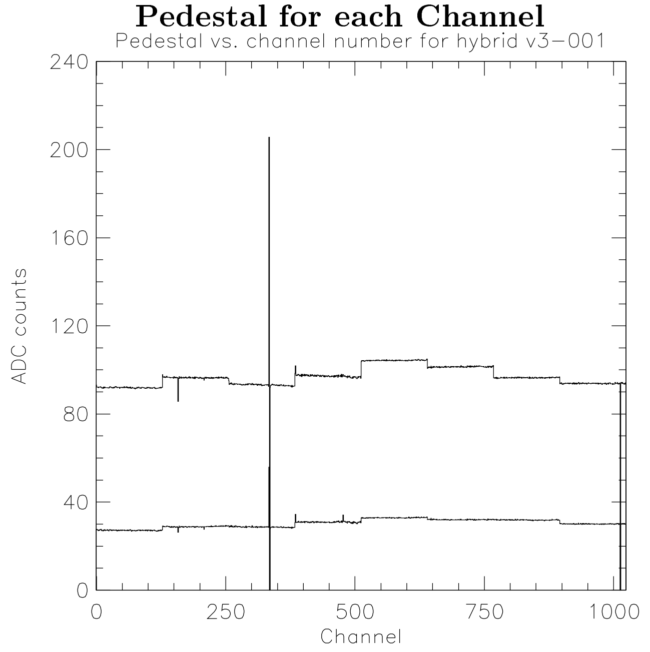
4 Comments

No comments.

5 Pedestal

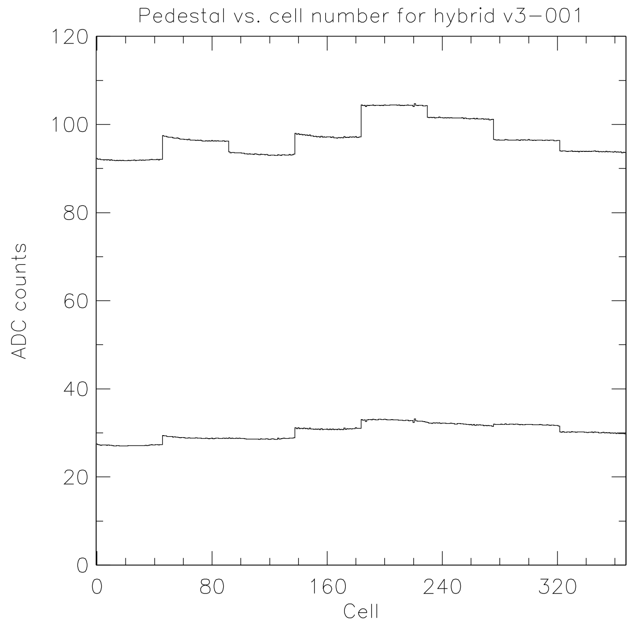
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

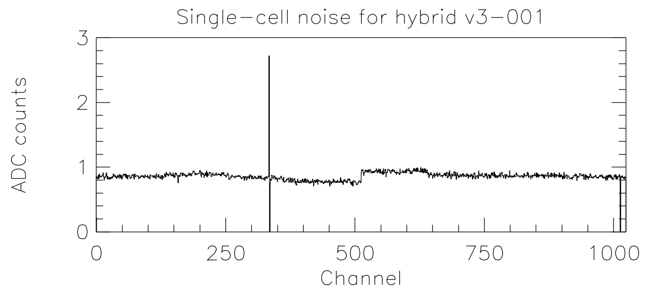
Pedestal vs. Pipeline Cell ID

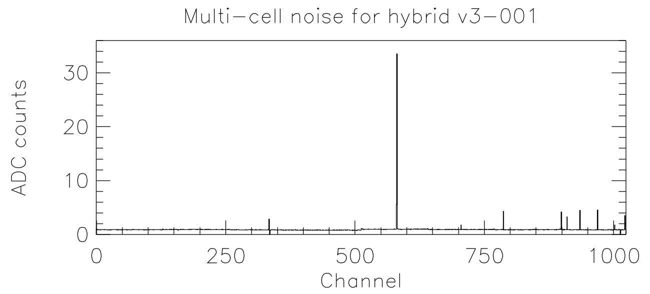


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

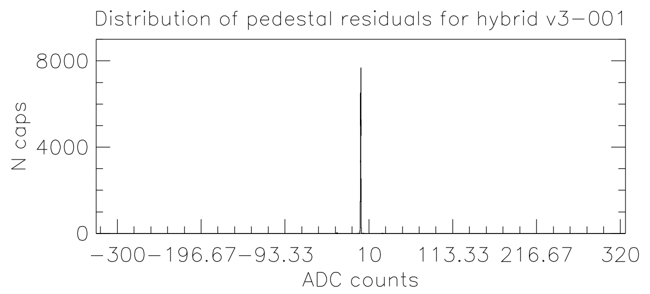
RMS Noise

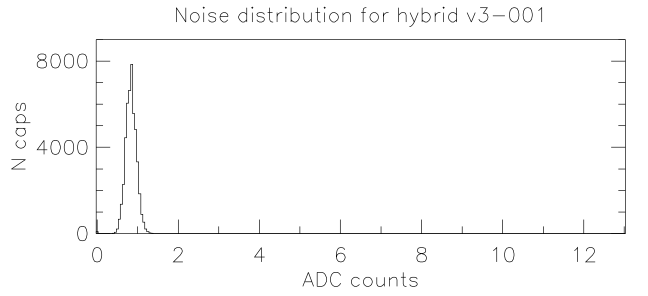




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in