# Hybrid 8j100 Traveler

January 31, 2000

## 1 Connectivity

Repairs on shorts:

Fixes for opens:

## 2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J100 has die: 038-036 101-051 043-003 038-045 099-041 099-042 099-045 099-046

## 3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j100 classification info. Created 10:41:20 01/26/00

Hybrid 8j100 quality: bad
Chip classification: bad good good fair good good fair good
Bad channels (chip-channel): 0-5 0-27 0-31 0-35 0-101 3-7
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-20-101 3-13-97 3-20-7
   6-4-73
Channels at pedestal needed for DCMS: 34.6 33.6 33.7 36.3 34.2 34.2 35.6 35.7
```

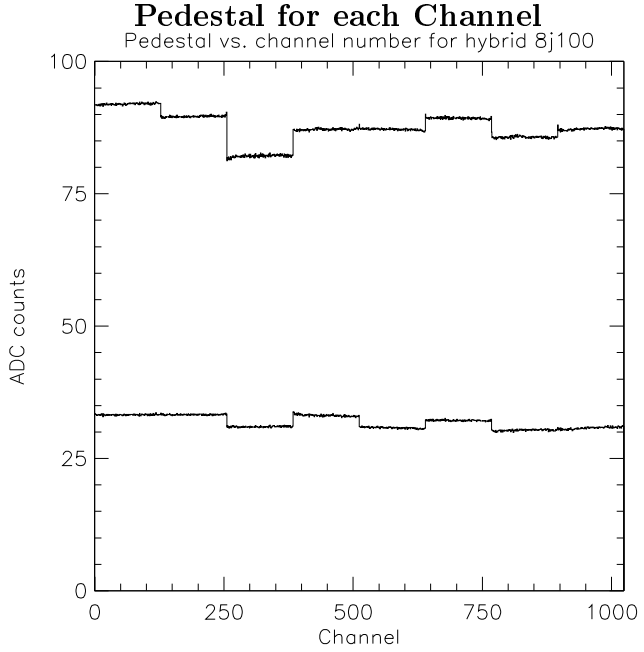
## 4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

# 5 Pedestal

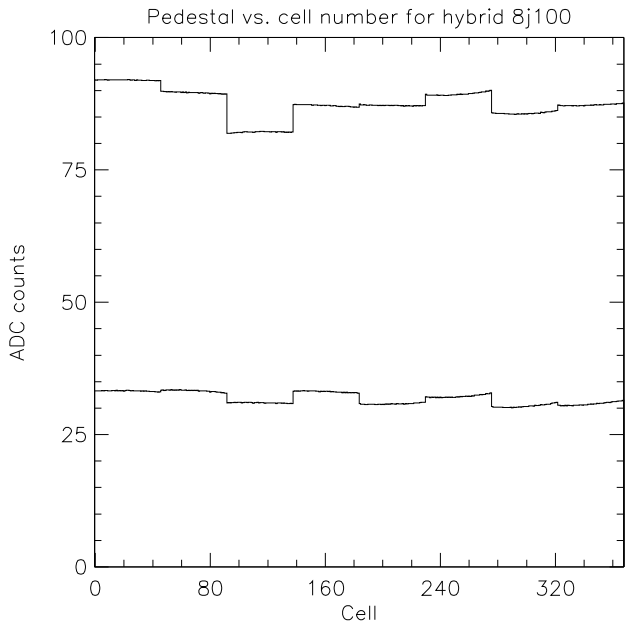
The following plot shows the pedestals vs. channel number with and without charge injection:

**Pedestal for each Channel**




The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

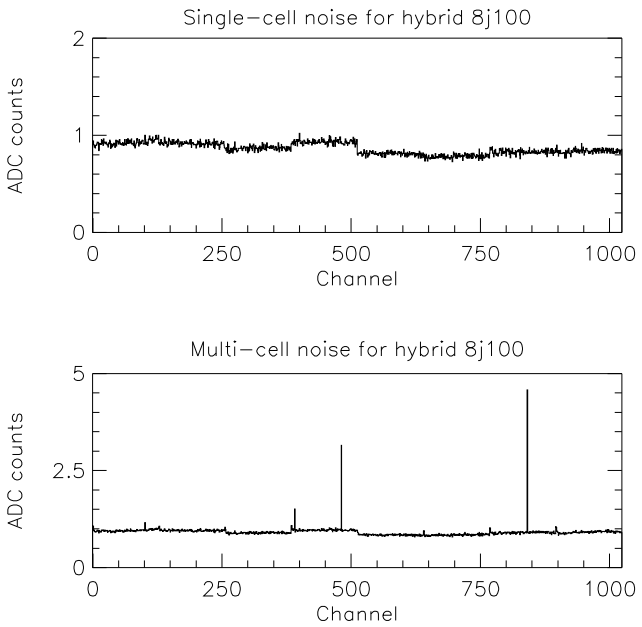
**Pedestal vs. Pipeline Cell ID**



# 6 Noise

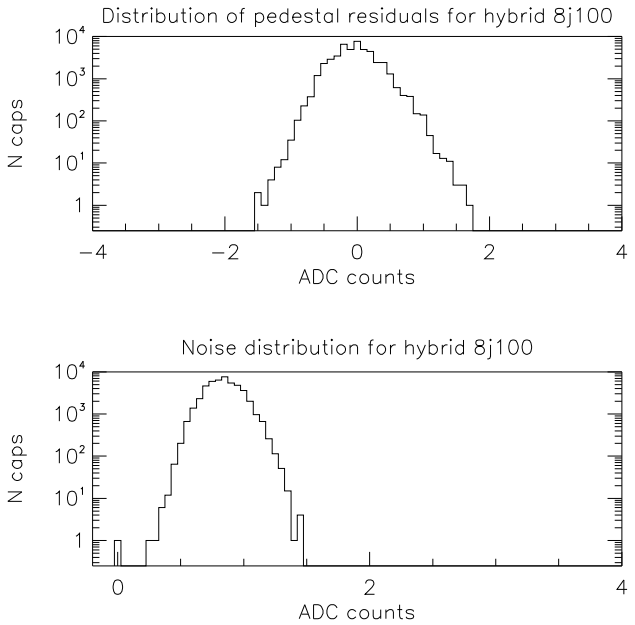
The following plots show the single-cell and multi-cell RMS noise:

**RMS Noise**

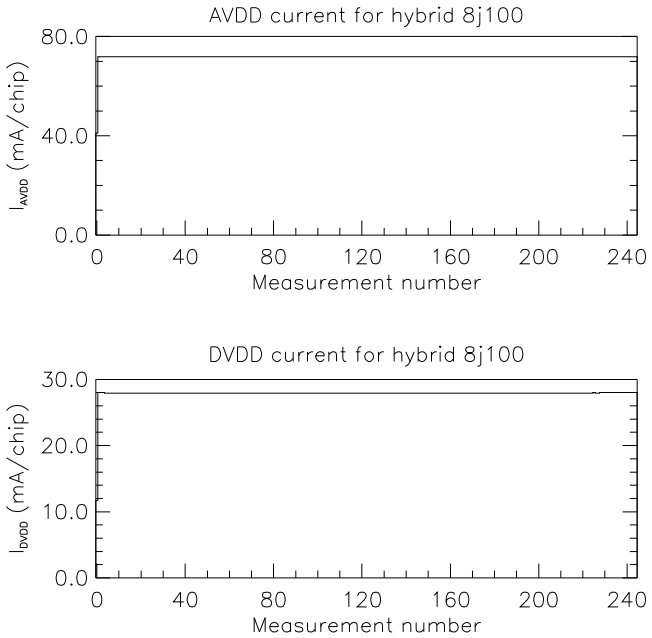



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

**Distribution of Pedestals and Noise**



# 7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

**Supply Currents During Burn-in**