Hybrid 8j105 Traveler

December 10, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J105 has die: 099-021 099-022 099-023 099-025 191-021 191-022 191-023 191-024

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j105 classification info. Created 15:20:03 12/01/99

Hybrid 8j105 quality: fair
Chip classification: good fair good good good good fair fair
Bad channels (chip-channel): 6-15 7-42
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-16-28 6-20-15
Channels at pedestal needed for DCMS: 35.7 35.6 35.6 35.6 30.6 31.3 31.2 30.4
```

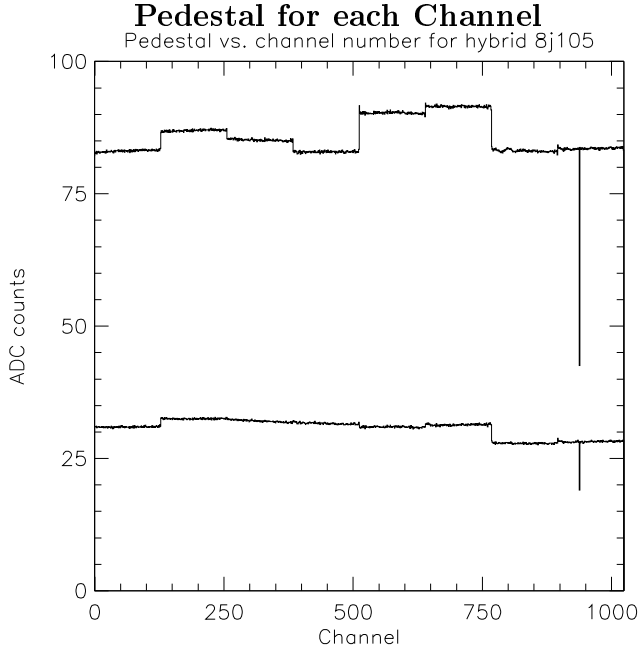
4 Comments

No comments.

5 Pedestal

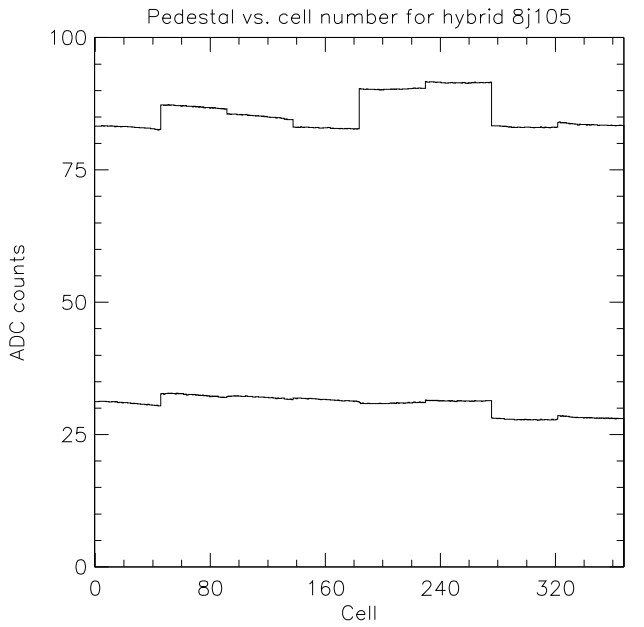
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

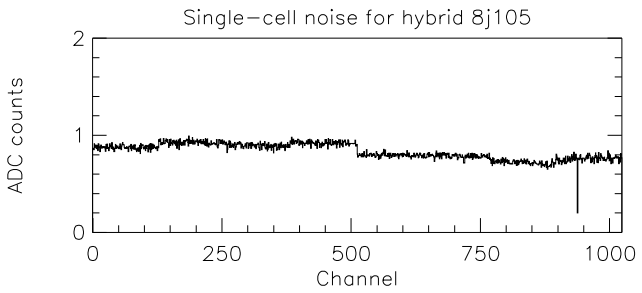
Pedestal vs. Pipeline Cell ID

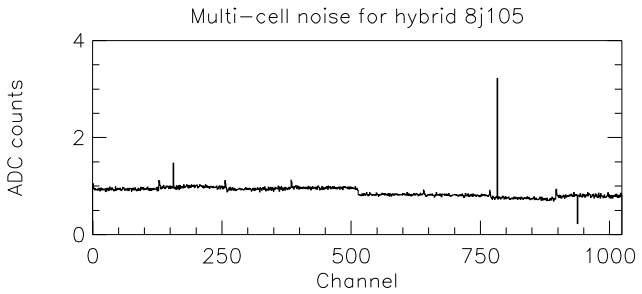


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

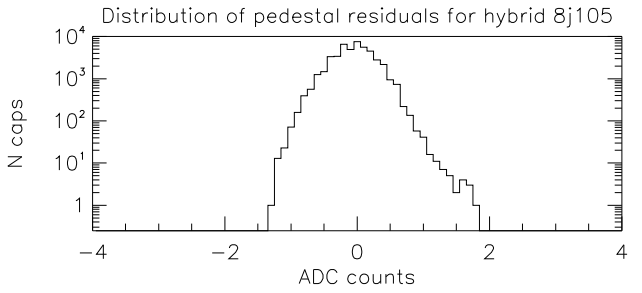
RMS Noise

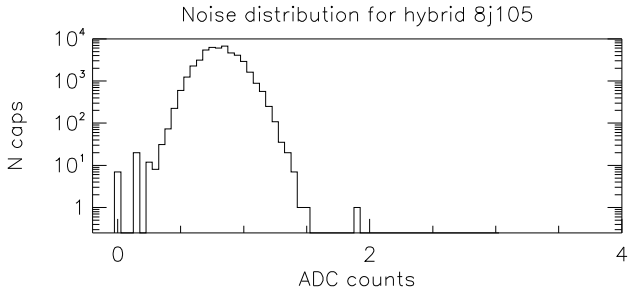




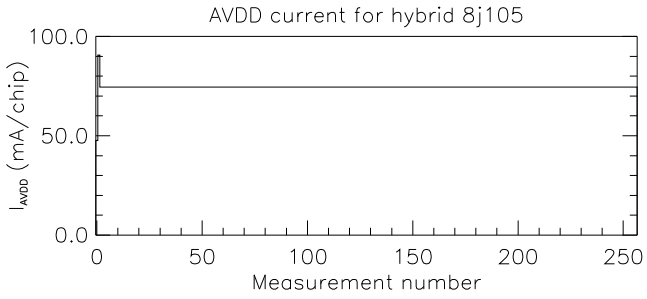
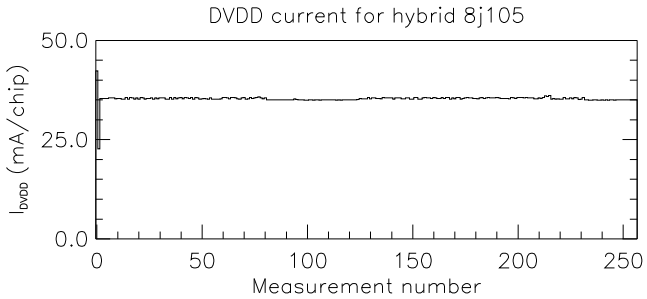
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in