Hybrid 8j115 Traveler

December 16, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J115 has die: 036-016 191-070 191-072 191-073 042-041 042-042 042-044 042-045

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j115 classification info. Created 09:56:09 12/13/99

Hybrid 8j115 quality: fair
Chip classification: fair good good good good fair good good
Bad channels (chip-channel): 0-53 0-54 5-44
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-0-52 0-10-52 0-18-52
   0-3-52 0-33-46 0-38-52 0-4-52
Channels at pedestal needed for DCMS: 33.6 33.6 32.4 33.6 33.5 33.0 34.6 36.6
```

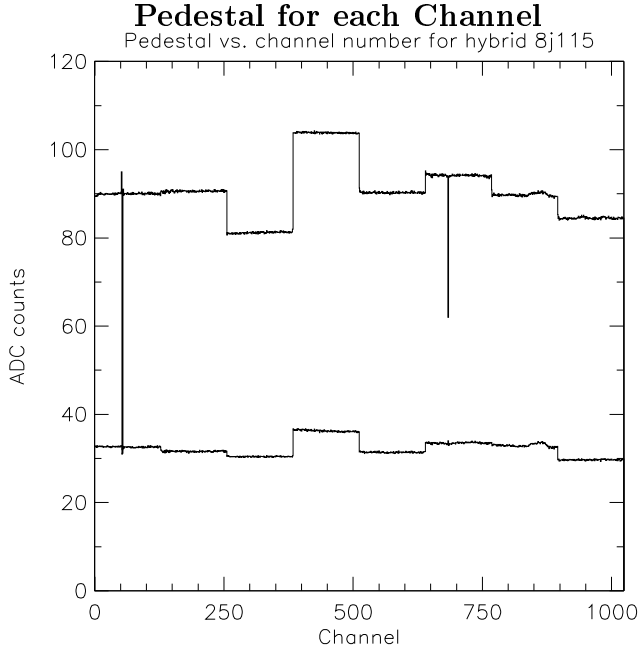
4 Comments

No comments.

5 Pedestal

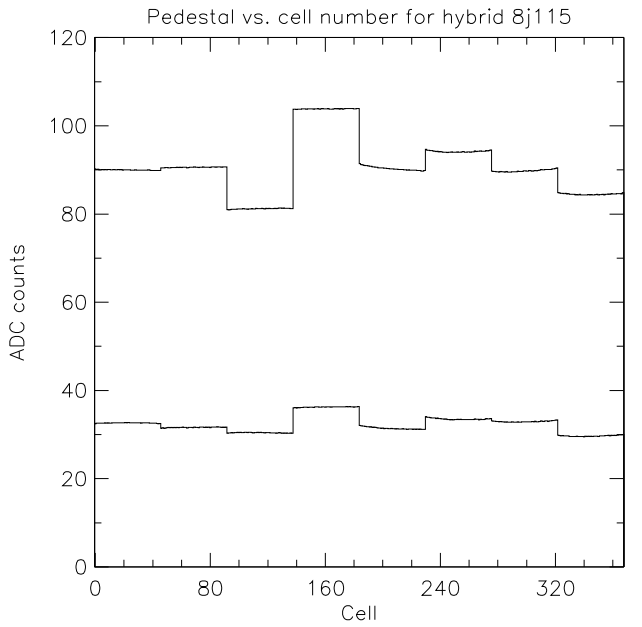
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

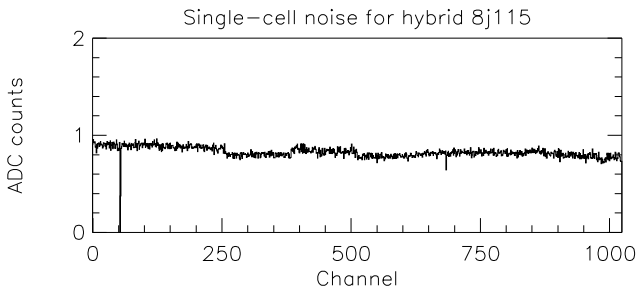
Pedestal vs. Pipeline Cell ID

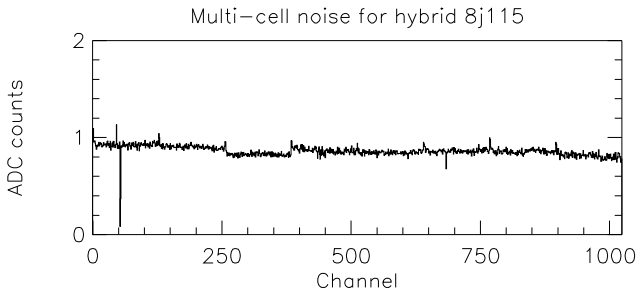


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

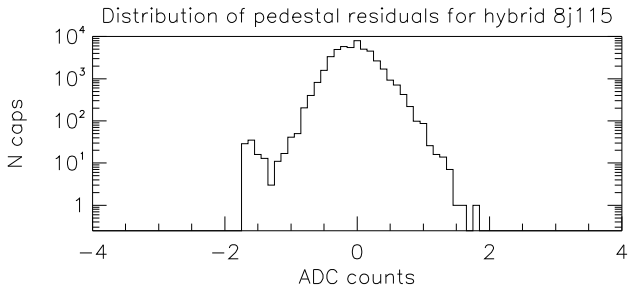
RMS Noise

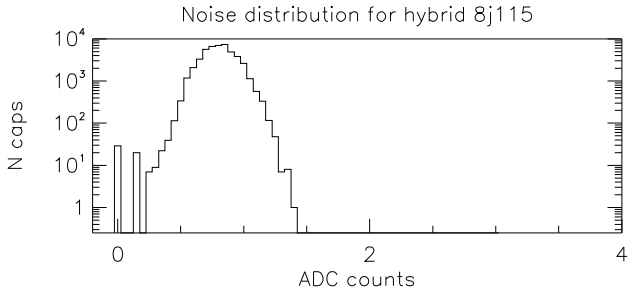




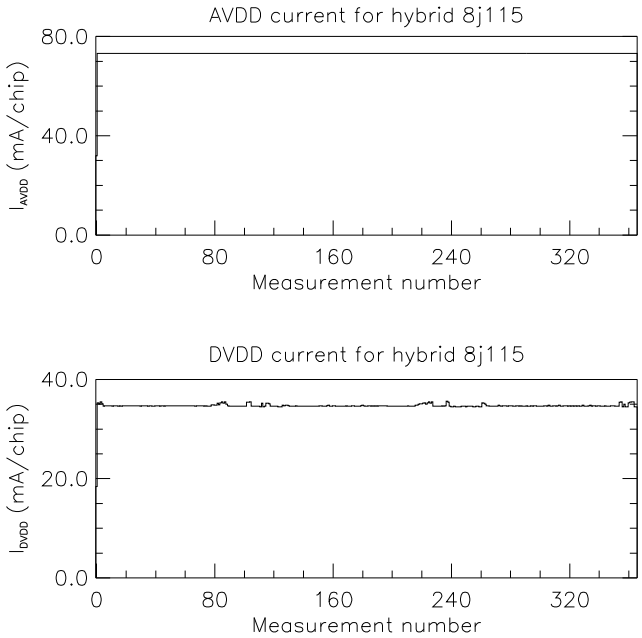
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in