Hybrid 8j133 Traveler

June 9, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J133 has die: 196-049 196-053 232-105 196-056 197-013 197-015 197-016 197-018

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j133 classification info. Created 09:21:52 06/07/00

Hybrid 8j133 quality: bad
Chip classification: fair fair fair good fair fair good bad
Bad channels (chip-channel): 0-66 1-99 2-86 7-111 7-112 7-116 7-117
Bad cells: none
Random bad capacitors (chip-cell-channel): 4-43-91 5-30-127
Channels at pedestal needed for DCMS: 30.8 29.7 31.6 31.6 30.4 30.6 30.6 28.8
```

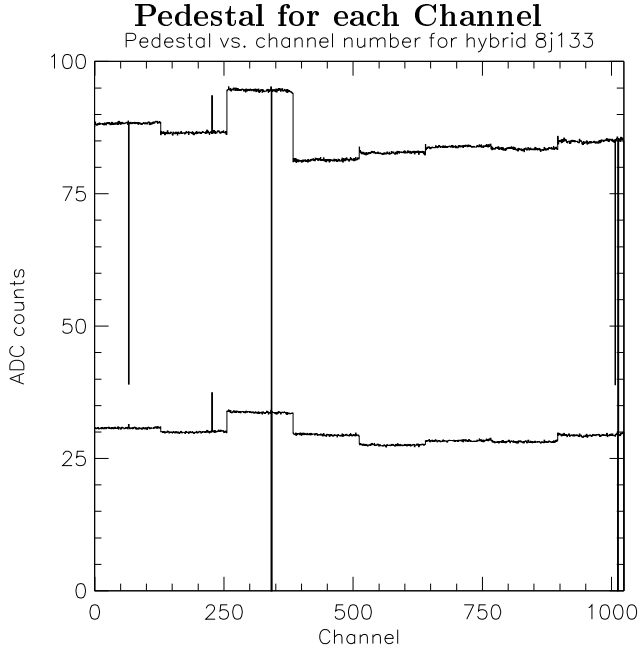
4 Comments

HV tested.

5 Pedestal

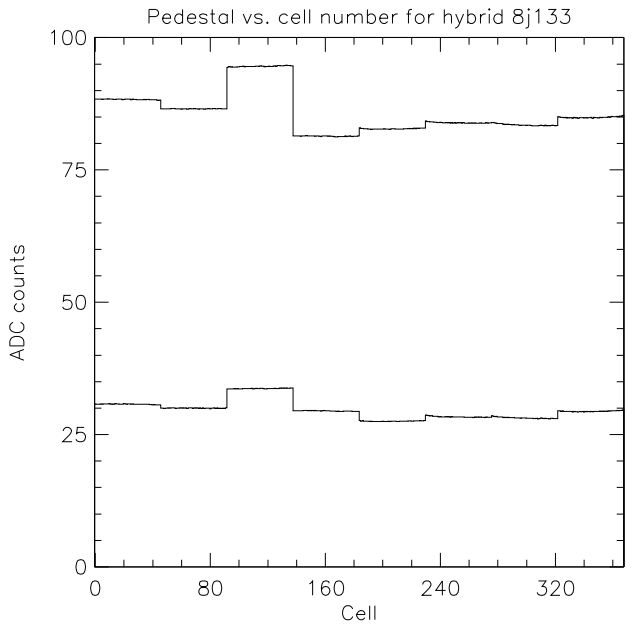
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

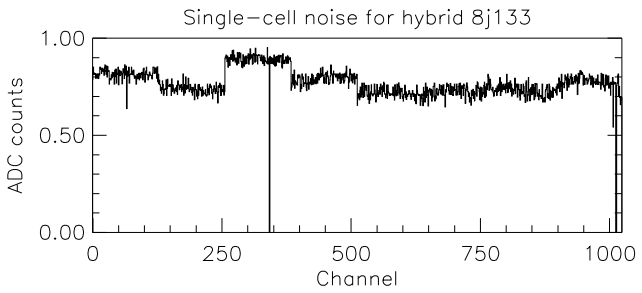
Pedestal vs. Pipeline Cell ID

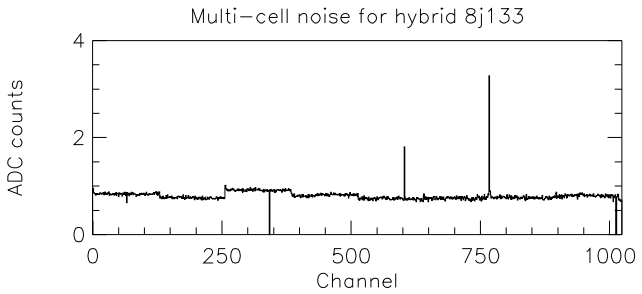


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

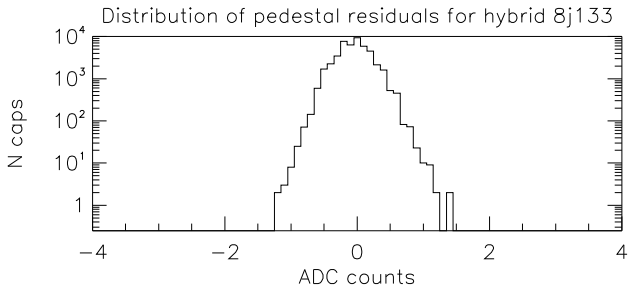
RMS Noise

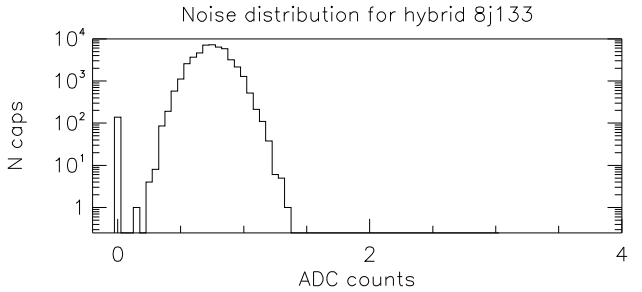




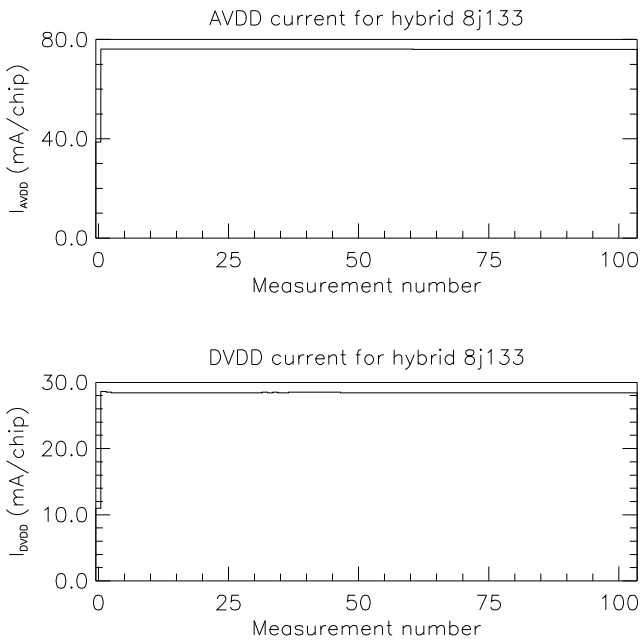
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in