Hybrid 8j16 Traveler

January 26, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J16 has die: 065-002 065-003 065-004 065-006 060-011 060-012 060-013 060-016

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid v3-016 classification info. Created 18:34:08 10/22/99

Hybrid v3-016 quality: bad
Chip classification: bad bad bad bad bad bad bad bad
Bad channels: N_bad_total = 1024 (too many to list all of them)
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-0-56 2-0-57 2-0-66 2-1-57 2-16-56 2-16-57 2-17-57 2-29-57 2-3-56 2-3-57 2-35-113 2-42-56 2-42-57 2-43-57 2-5-56 2-5-57 2-7-56 2-7-57 3-7-127 7-21-88
Channels at pedestal needed for DCMS: 33.3 35.2 34.7 34.1 36.6 36.6 38.3 38.6
```

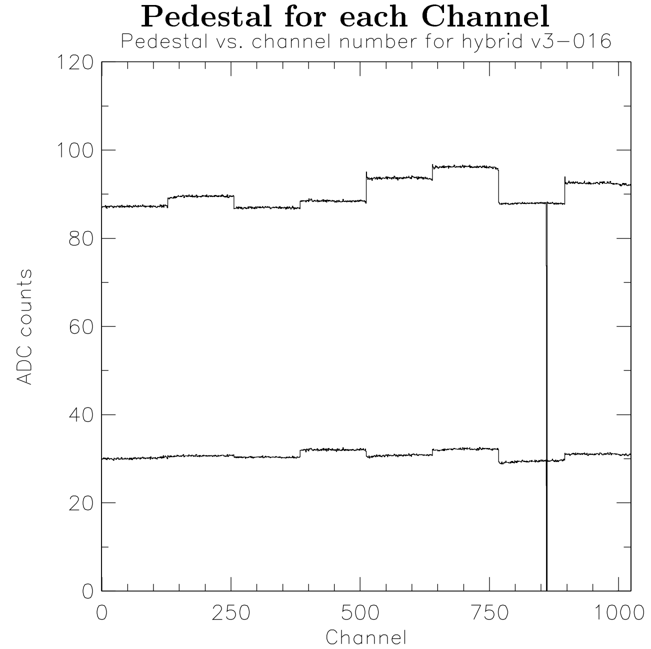
4 Comments

No comments. Some bad channels. Judged OKAY.

5 Pedestal

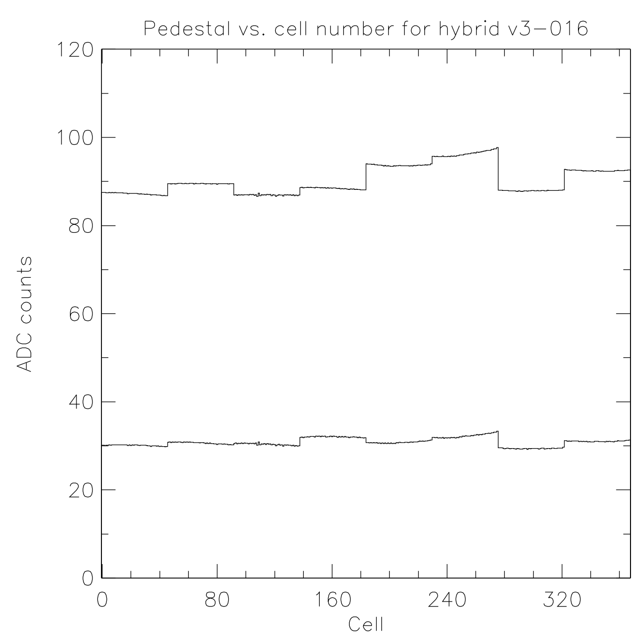
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

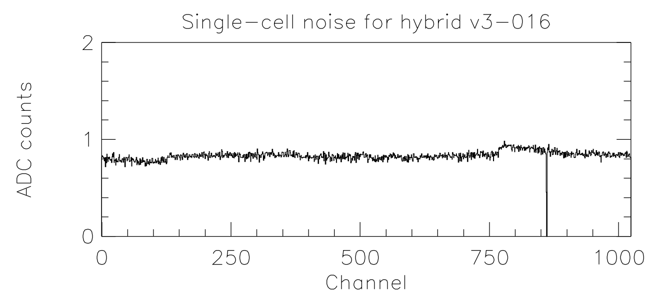
Pedestal vs. Pipeline Cell ID

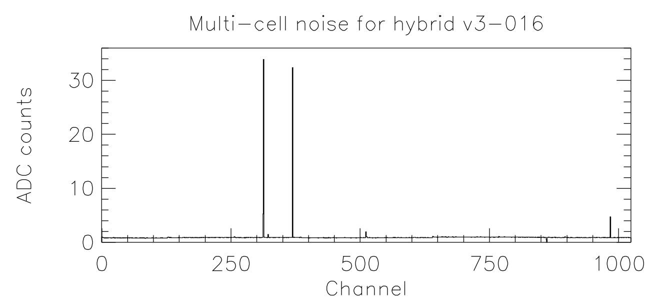


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

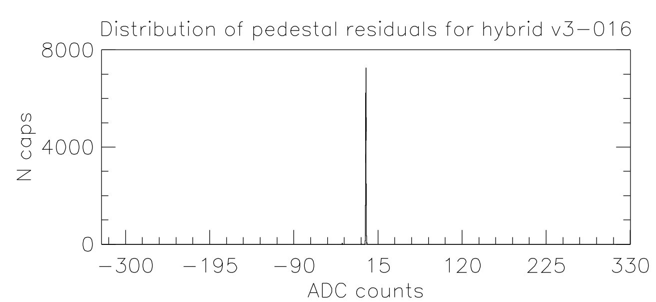
RMS Noise

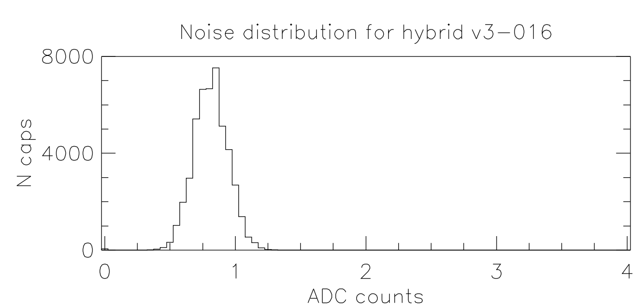




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in