Hybrid 8j173 Traveler

March 8, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J173 has die: 204-100 204-104 204-105 204-106 211-120 187-016 211-122 211-125

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j173 classification info. Created 09:53:06 03/08/00

Hybrid 8j173 quality: fair
Chip classification: fair good fair fair good fair fair fair
Bad channels (chip-channel): 0-93 3-94 5-70 6-27 6-83 7-12
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-31-68 6-24-61 6-24-62
   6-26-57 7-11-23 7-18-126 7-32-126 7-38-126 7-40-126 7-42-126 7-5-126
   7-5-127 7-6-126
Channels at pedestal needed for DCMS: 31.1 34.6 33.6 34.5 32.6 32.6 31.5 32.7
```

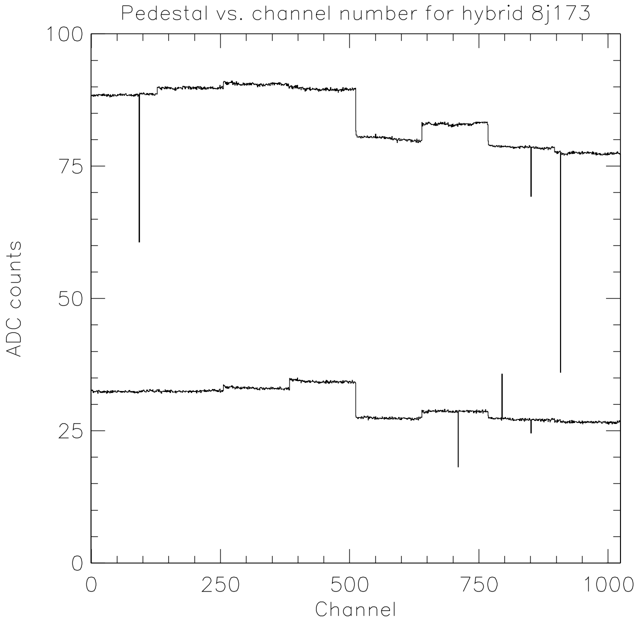
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

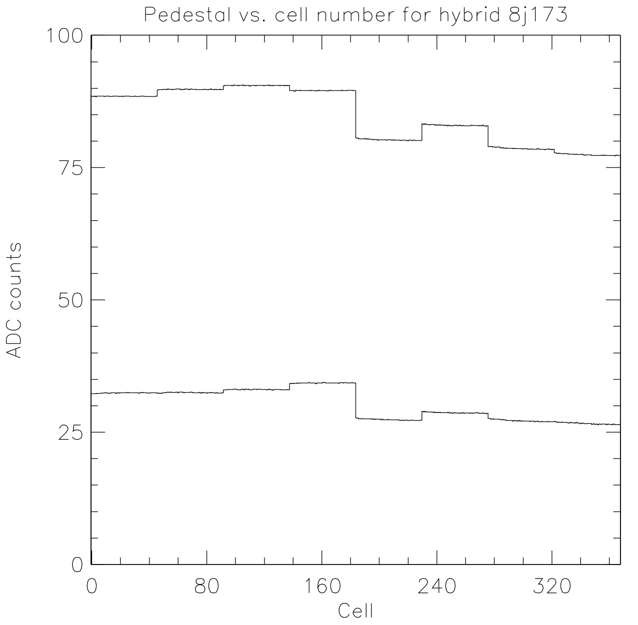
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

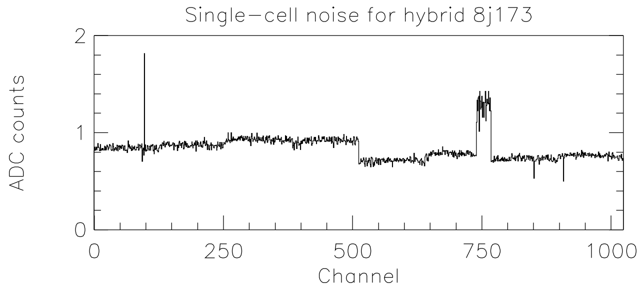
Pedestal vs. Pipeline Cell ID

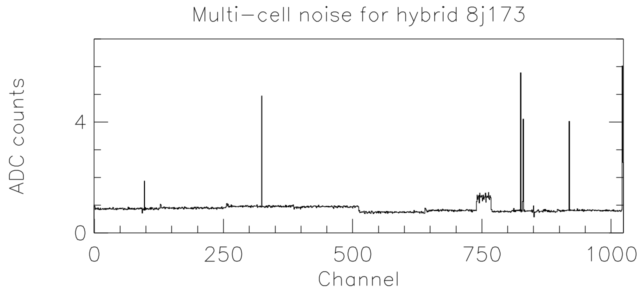


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

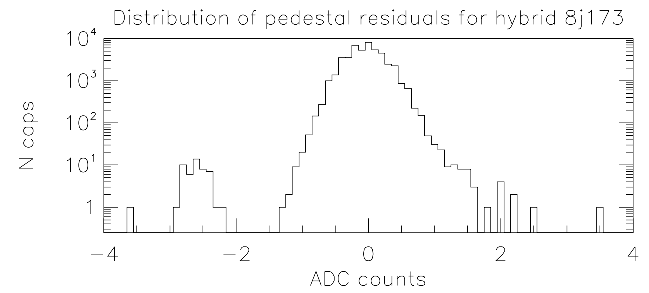
RMS Noise

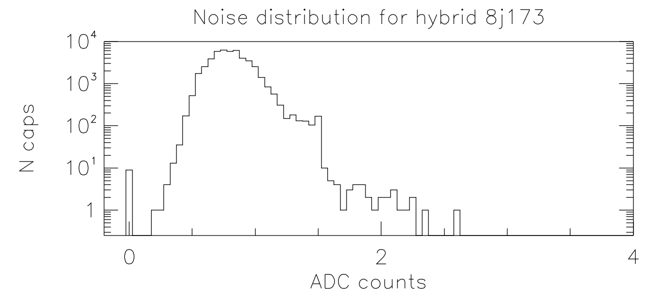




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in