Hybrid 8j176 Traveler

January 26, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J176 has die: 204-117 204-120 204-121 204-123 187-017 187-018 187-020 187-022

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j176 classification info. Created 16:08:47 01/20/00

Hybrid 8j176 quality: bad
Chip classification: good good good good fair fair bad fair
Bad channels (chip-channel): 4-27 4-96 5-67 6-79 7-29 7-99
Bad cells: none
Random bad capacitors (chip-cell-channel): 4-29-83 7-19-29 7-26-29
   7-27-29 7-28-29 7-29-29 7-36-29 7-37-29 7-42-29
Channels at pedestal needed for DCMS: 32.6 33.6 33.6 32.6 30.7 31.6 31.8 31.4
```

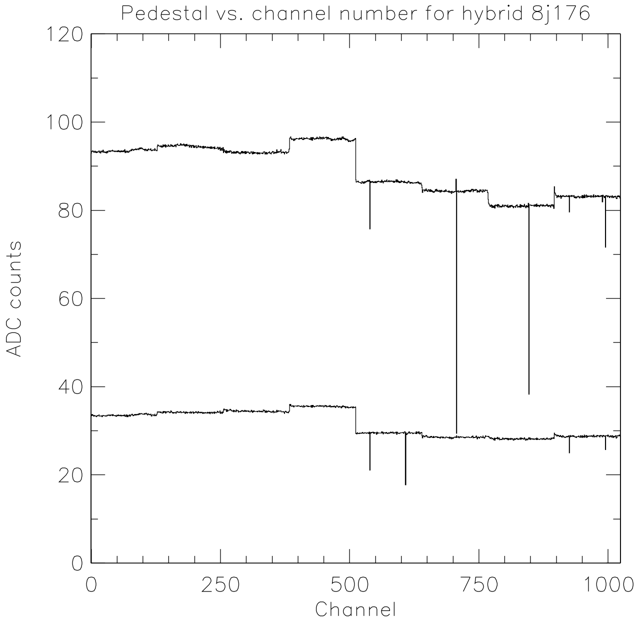
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested. Passed post burn-in considerations (htest). Okay

5 Pedestal

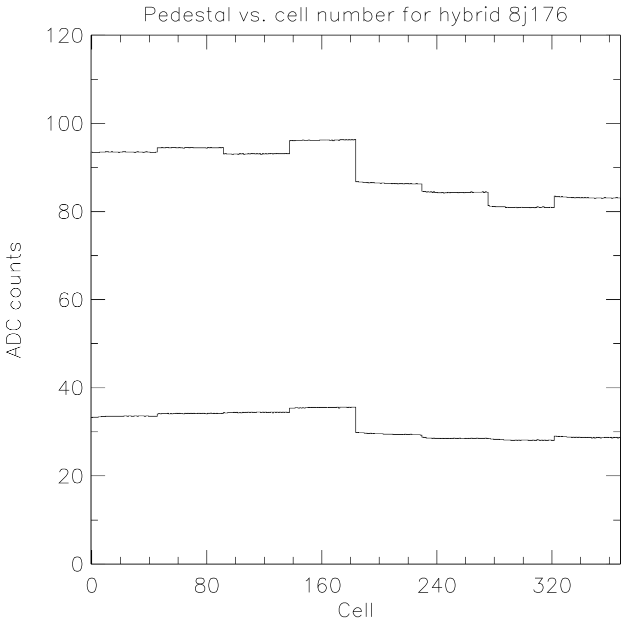
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

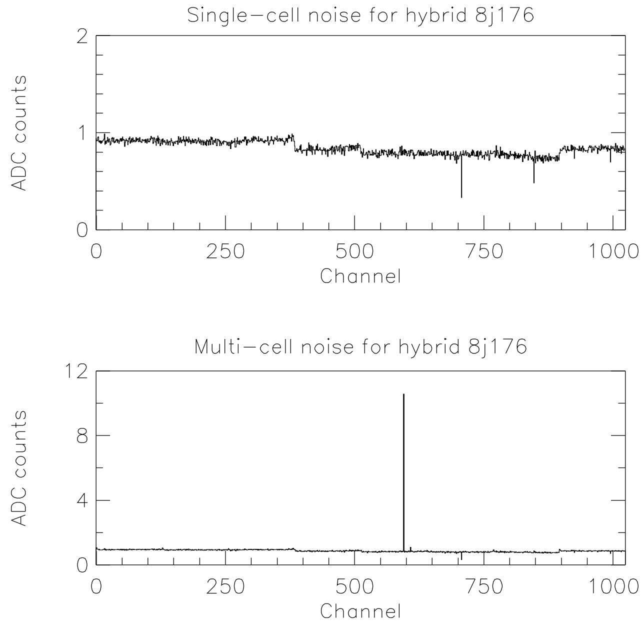
Pedestal vs. Pipeline Cell ID



6 Noise

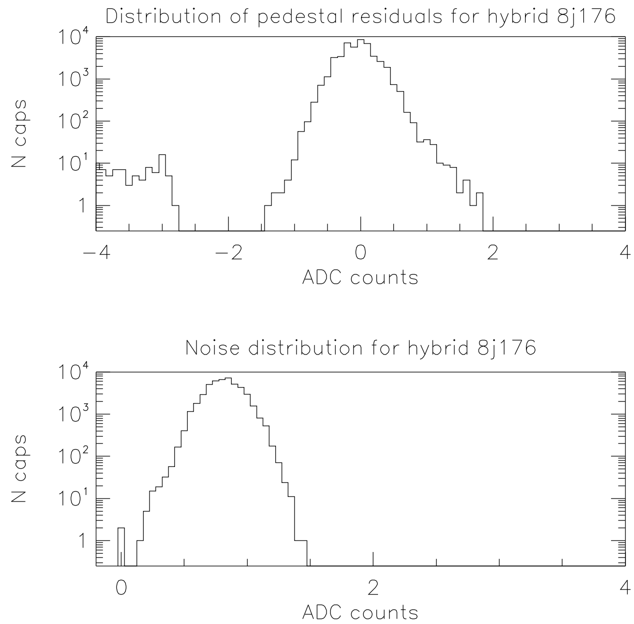
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in