Hybrid 8j180 Traveler

July 27, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J180 has die: 187-050 187-053 187-054 159-086 187-095 229-124 229-125 229-126

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

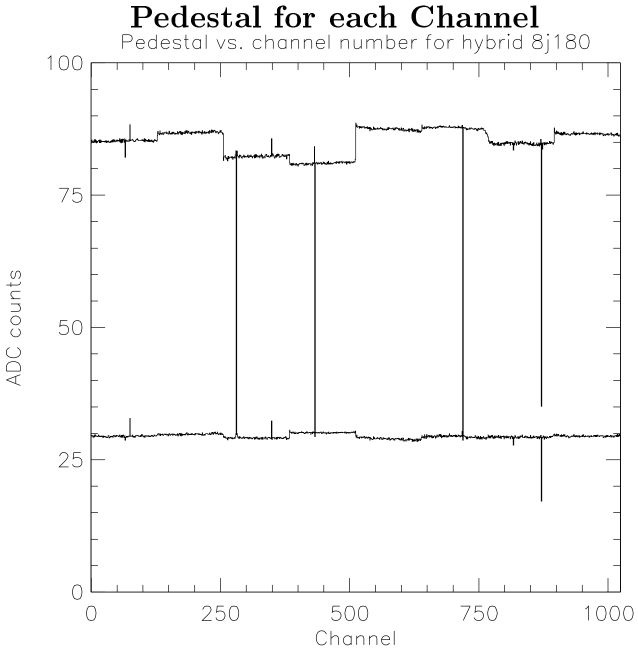
```
% Hybrid 8j180 classification info. Created 09:15:05 06/05/00

Hybrid 8j180 quality: fair
Chip classification: fair fair fair fair fair fair fair good
Bad channels (chip-channel): 0-61 2-25 3-49 4-33 4-47 5-79 6-103
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-20-61 0-33-64 1-32-101
   4-1-56 4-1-57 4-14-56 4-14-57 4-2-57 4-27-56 4-27-57 4-31-56
   4-31-57 4-34-56 4-34-57 4-36-56 4-36-57 4-38-56 4-38-57 5-45-53
Channels at pedestal needed for DCMS: 31.6 34.2 33.7 31.7 33.6 32.6 33.6 35.7
```

4 Comments

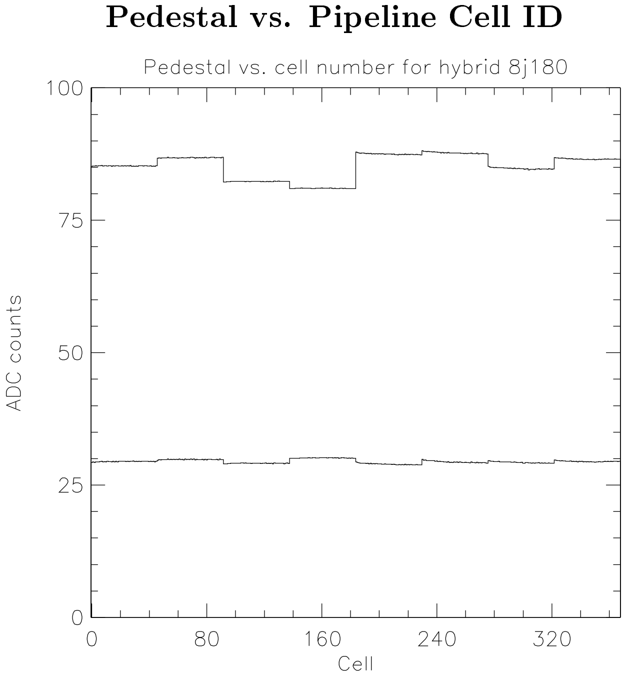
HV tested.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



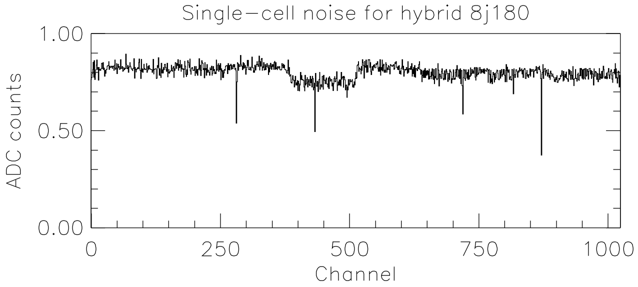
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

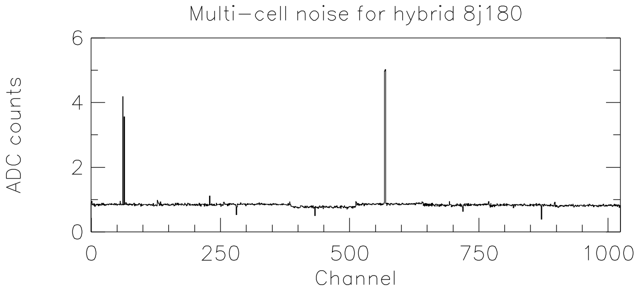


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

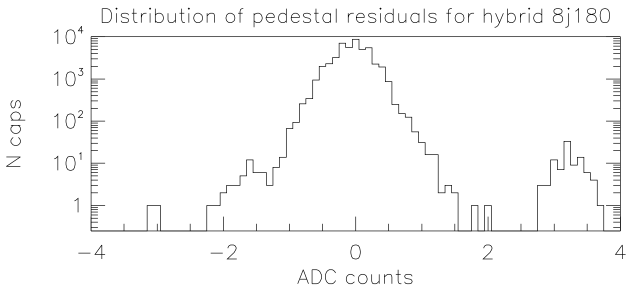
RMS Noise

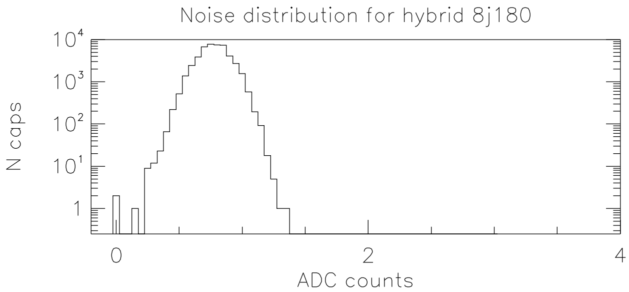




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in