Hybrid 8j184 Traveler

January 26, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J184 has die: 187-086 187-088 187-090 187-093 228-018 228-020 228-021 228-022

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

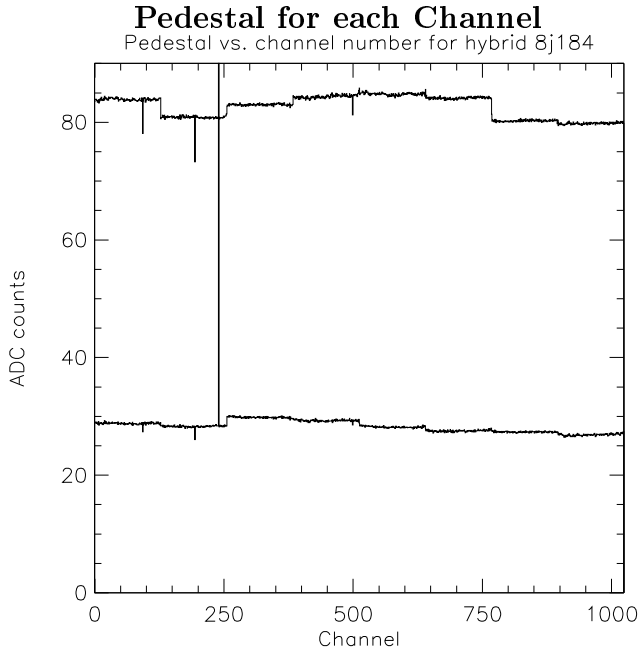
```
% Hybrid 8j184 classification info. Created 11:22:38 01/24/00

Hybrid 8j184 quality: fair
Chip classification: good fair good good good good good good
Bad channels (chip-channel): 1-66 1-112
Bad cells: none
Random bad capacitors: none
Channels at pedestal needed for DCMS: 34.5 34.6 35.6 35.6 31.3 31.6 30.7 31.5
```

4 Comments

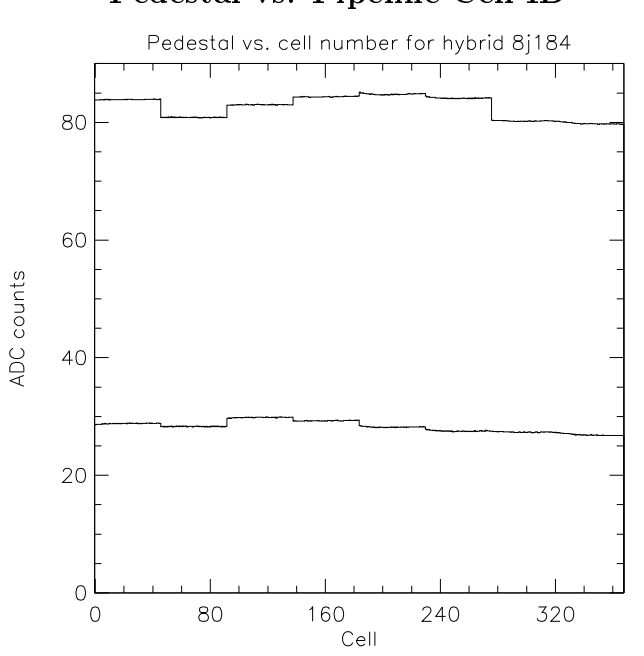
Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



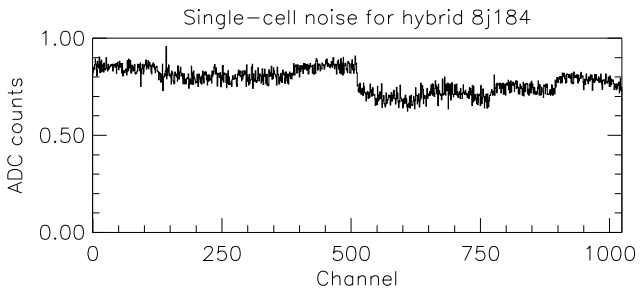
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

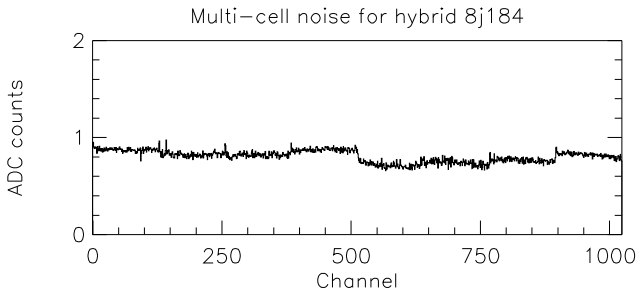


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

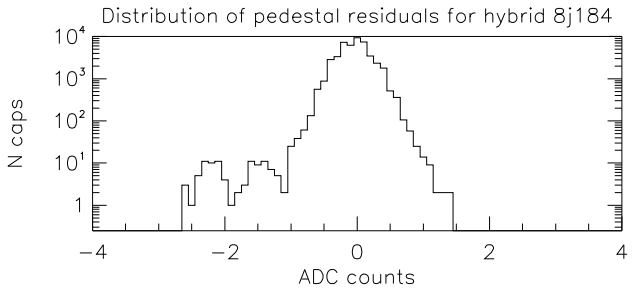
RMS Noise

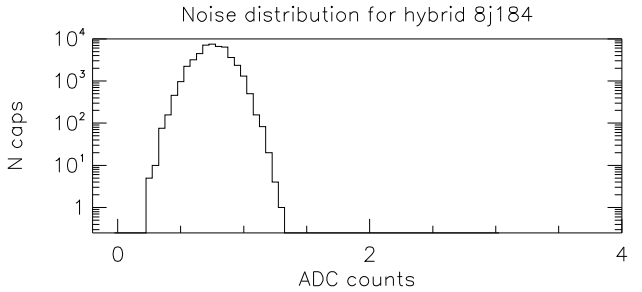




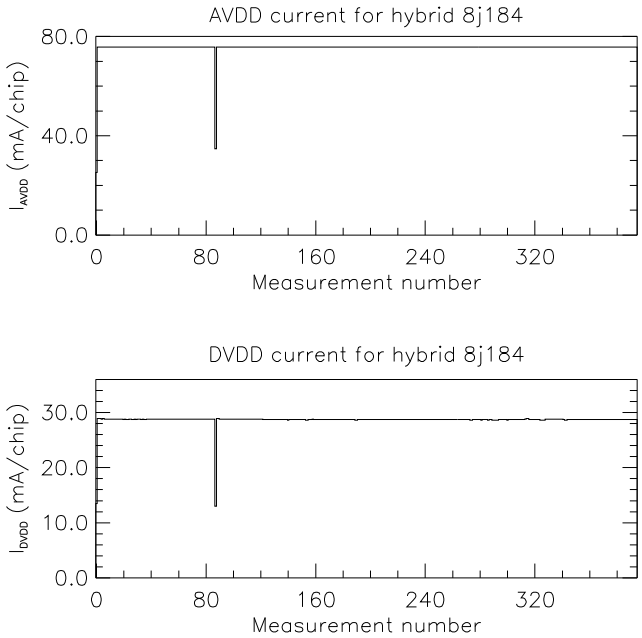
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in