Hybrid 8j185 Traveler

January 26, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J185 has die: 228-024 228-026 228-027 228-028 228-054 228-055 228-056 228-057

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j185 classification info. Created 11:00:58 01/24/00

Hybrid 8j185 quality: fair
Chip classification: good good fair good good good good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-1-116 2-1-117 2-14-117
   2-15-116 2-15-117 2-16-116 2-16-117 2-2-116 2-2-117 2-27-117 2-28-117
   2-3-116 2-3-117 2-32-117 2-34-117 2-36-117 2-4-117 2-5-117
Channels at pedestal needed for DCMS: 29.7 31.6 31.7 31.7 33.6 32.6 32.7 32.4
```

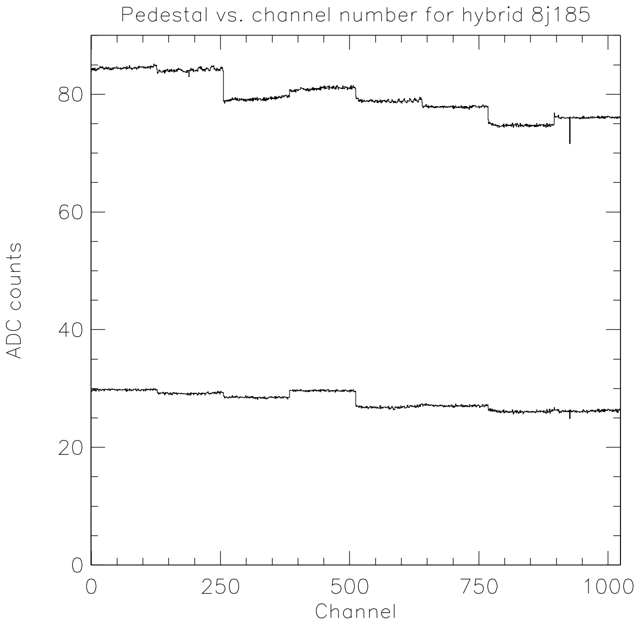
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

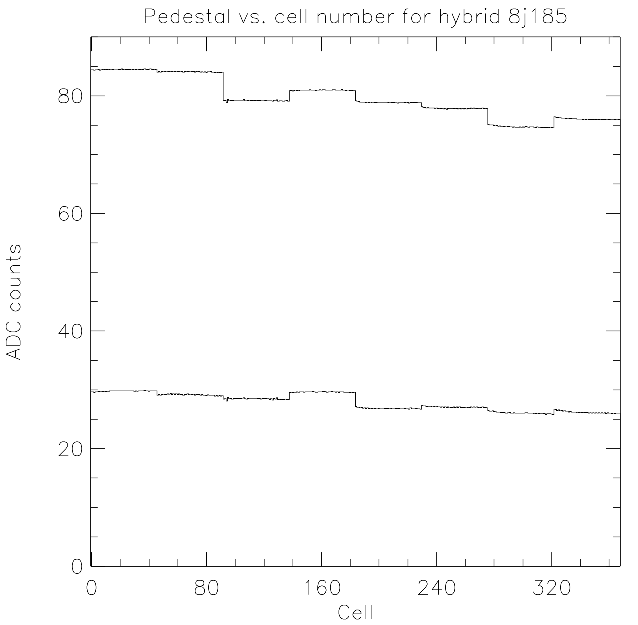
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

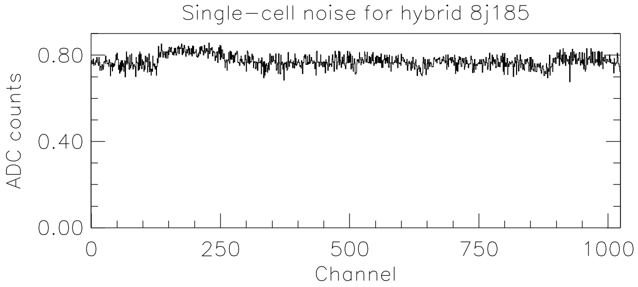
Pedestal vs. Pipeline Cell ID

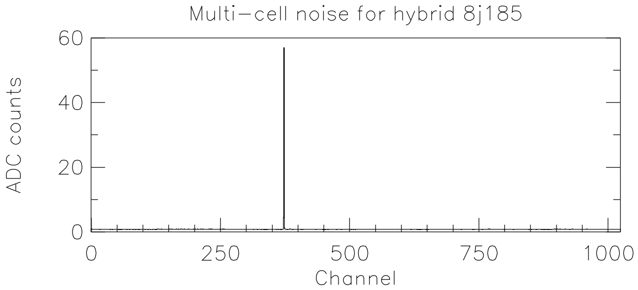


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

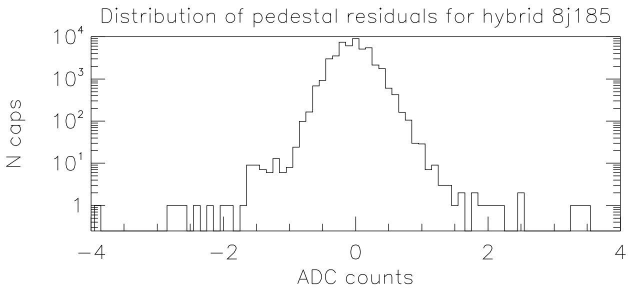
RMS Noise

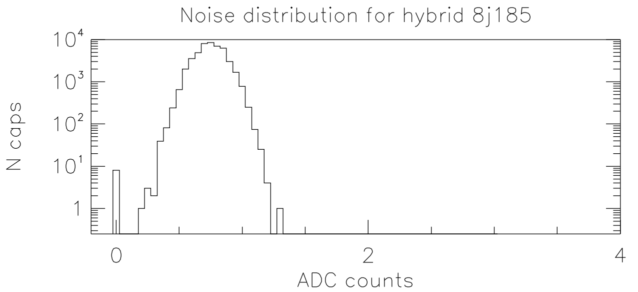




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in