Hybrid 8j194 Traveler

February 7, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J194 has die: 228-100 228-105 228-106 228-107 227-030 227-031 227-036 227-037

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j194 classification info. Created 10:46:08 02/07/00

Hybrid 8j194 quality: fair
Chip classification: fair good good good good fair fair good
Bad channels (chip-channel): 0-3 5-73
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-15-3 0-16-3 0-17-3
   0-18-3 0-19-3 0-20-3 0-21-3 0-22-3 0-24-3 0-25-3 0-26-3
   0-35-3 0-39-17 0-42-28 0-44-35 0-45-38 0-45-39 6-39-99
Channels at pedestal needed for DCMS: 32.6 31.6 33.6 33.6 30.7 29.7 32.7 32.5
```

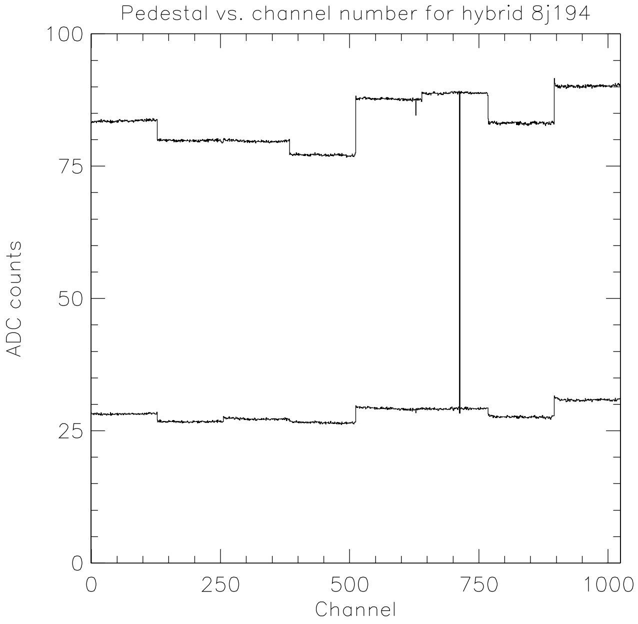
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

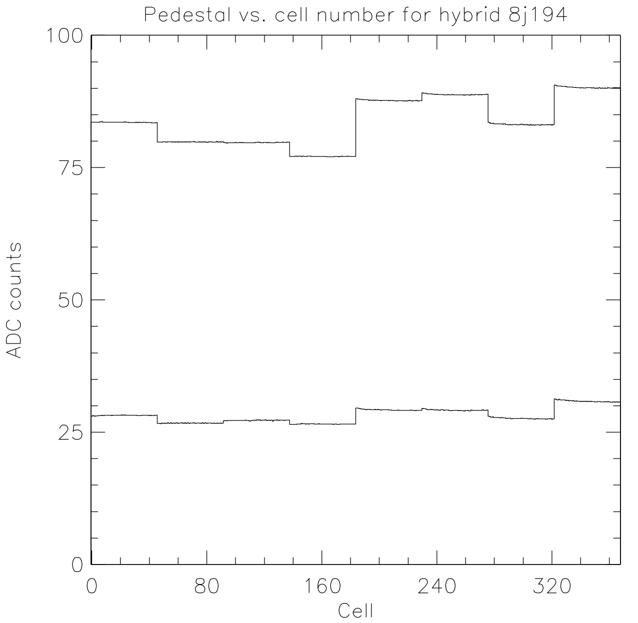
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

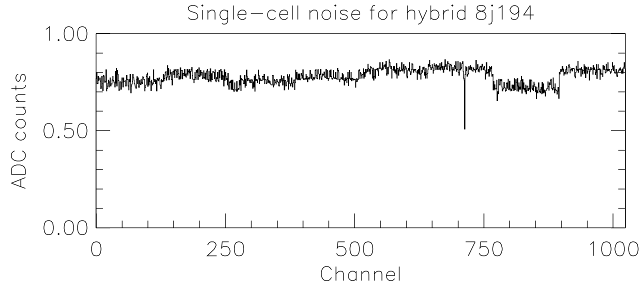
Pedestal vs. Pipeline Cell ID

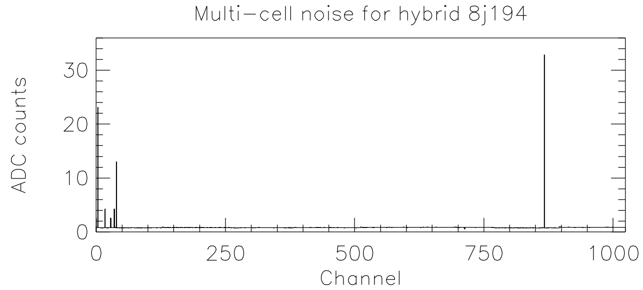


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

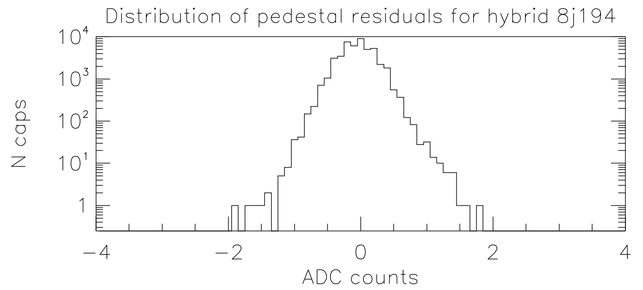
RMS Noise

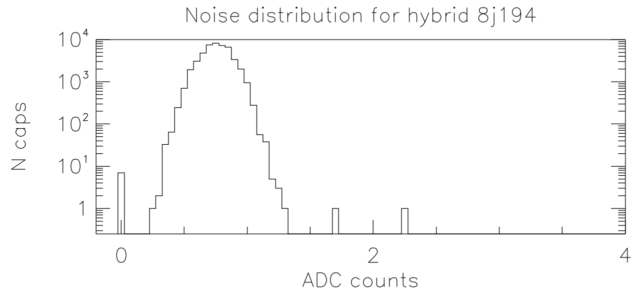




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in