Hybrid 8j195 Traveler

February 2, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J195 has die: 000-000 000-000 000-000 000-000 000-000 000-000 000-000 000-000

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j195 classification info. Created 11:43:15 02/02/00

Hybrid 8j195 quality: fair
Chip classification: good fair good fair good fair good fair
Bad channels (chip-channel): 1-86 5-70
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-35-122 3-10-63 3-12-63
   3-13-63 3-15-63 3-17-63 3-19-63 3-2-63 3-20-63 3-21-63 3-23-63
   3-25-63 3-26-63 3-27-63 3-28-63 3-3-63 3-32-63 3-34-63 3-35-63
   3-36-63 3-37-63 3-39-63 3-4-63 3-45-63 3-5-63 3-6-63 3-8-63
   3-9-63 7-18-22
Channels at pedestal needed for DCMS: 33.7 31.6 34.6 32.6 30.7 31.6 32.7 31.6
```

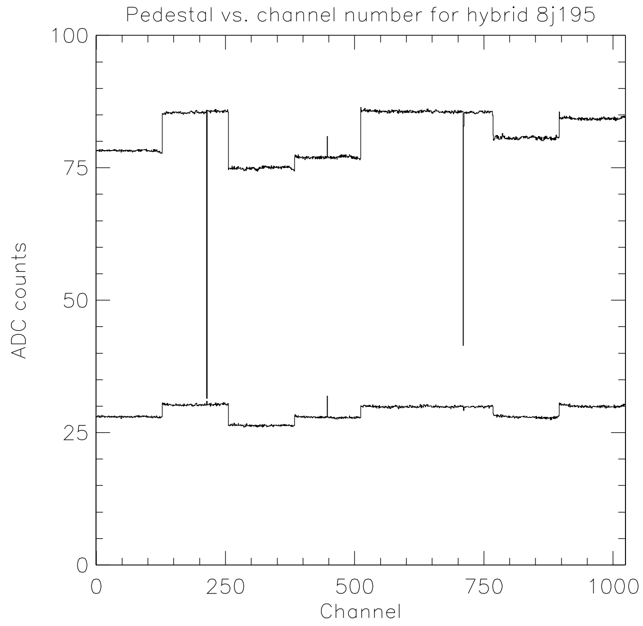
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

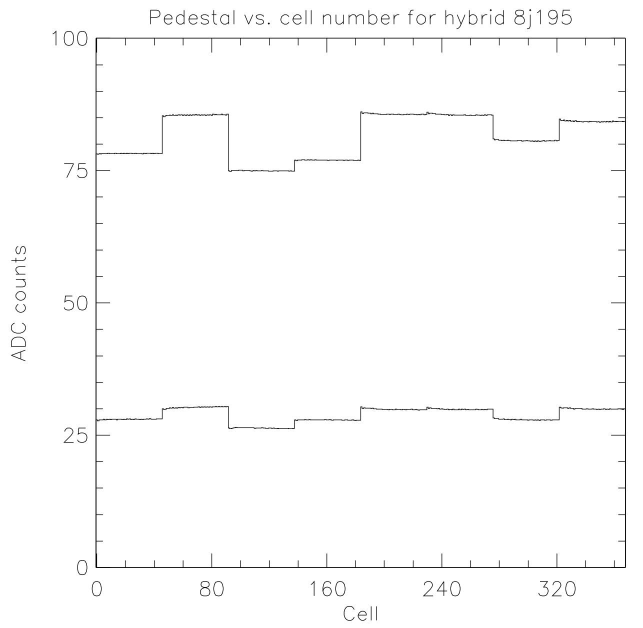
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

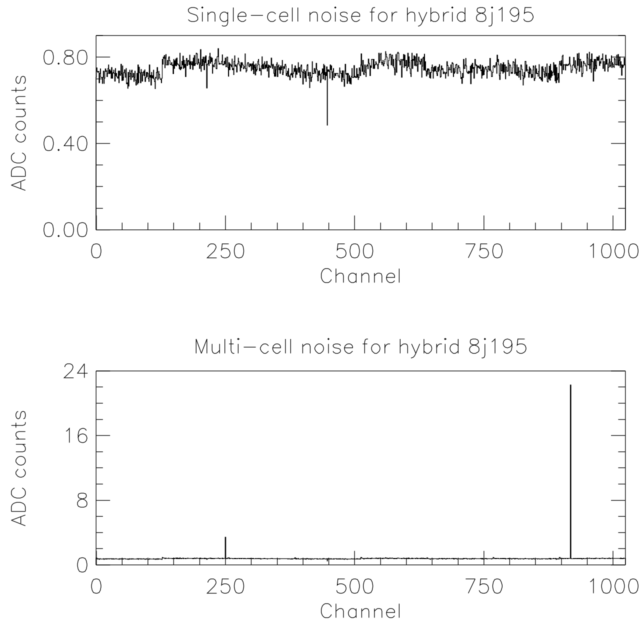
Pedestal vs. Pipeline Cell ID



6 Noise

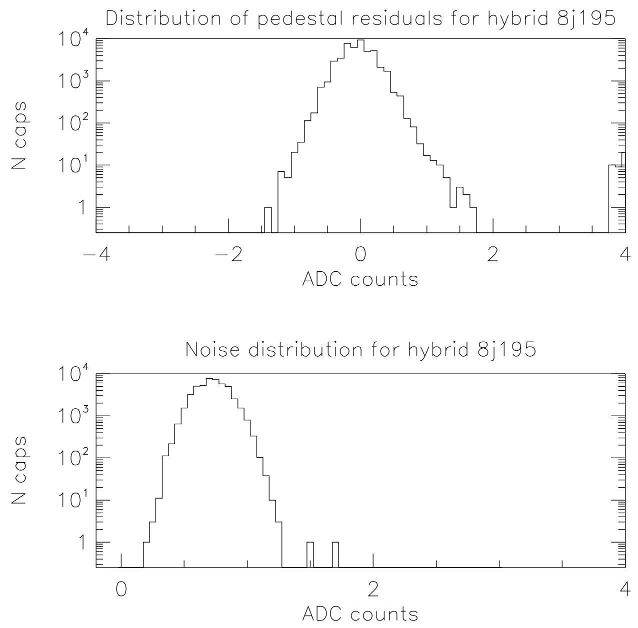
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in