Hybrid 8j201 Traveler

February 15, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J201 has die: 177-027 177-028 177-030 177-031 177-082 177-085 177-089 177-090

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j201 classification info. Created 09:52:06 02/14/00

Hybrid 8j201 quality: fair
Chip classification: fair good fair fair good good fair good
Bad channels (chip-channel): 3-2
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-10-116 0-13-116 0-13-117
   0-14-116 0-16-116 0-16-117 0-18-116 0-18-117 0-20-116 0-20-117 0-29-116
   0-29-117 0-30-116 0-42-116 0-9-116 0-9-117 2-12-53 2-36-77 2-37-44
   6-25-45 6-25-7 6-25-98 6-40-115
Channels at pedestal needed for DCMS: 32.3 32.6 32.7 31.7 32.9 31.6 34.7 33.7
```

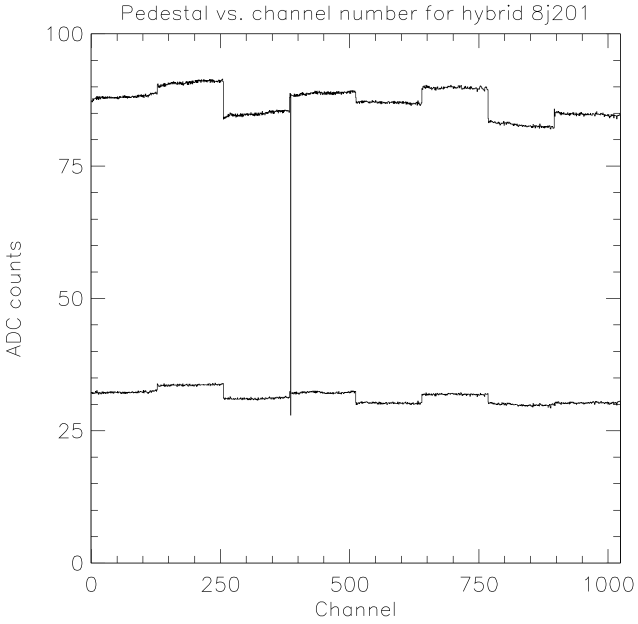
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

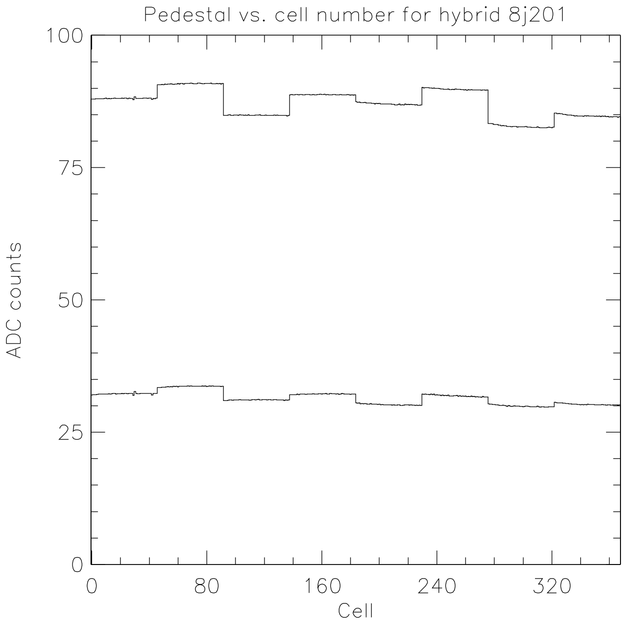
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

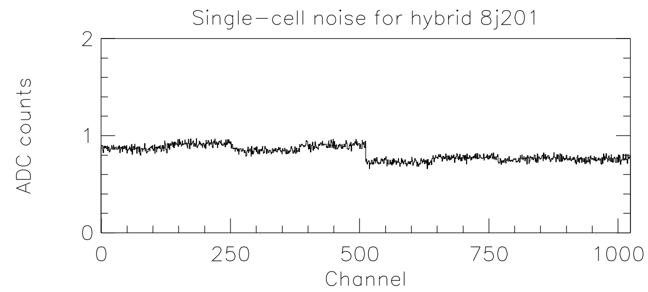
Pedestal vs. Pipeline Cell ID

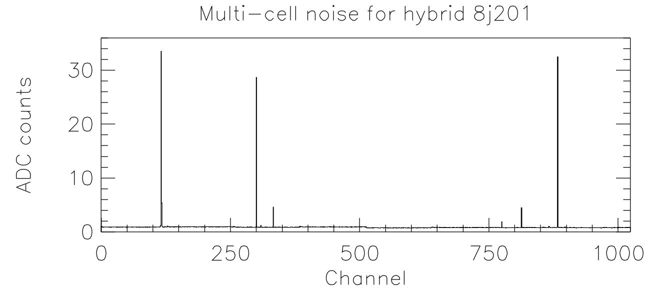


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

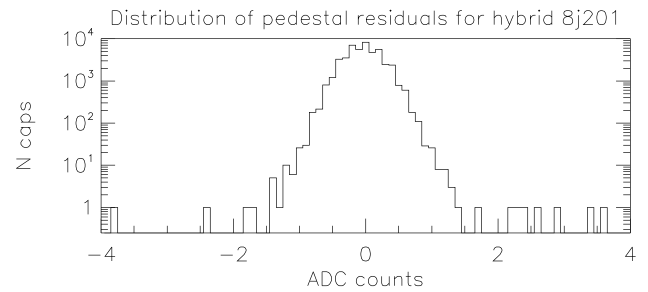
RMS Noise

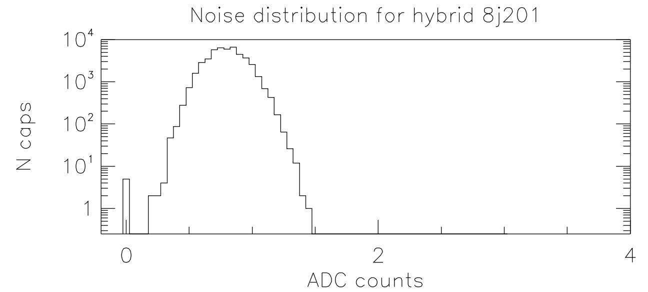




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in