Hybrid 8j203 Traveler

February 7, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J203 has die: 177-095 177-096 177-097 177-098 179-078 179-079 179-083 179-084

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j203 classification info. Created 09:51:47 02/07/00

Hybrid 8j203 quality: fair
Chip classification: good fair fair good fair good good good
Bad channels (chip-channel): 2-109
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-25-114 1-36-41 1-44-96
   2-29-110 2-41-115 2-41-117 4-25-123 4-25-124
Channels at pedestal needed for DCMS: 34.7 34.7 33.6 33.6 34.5 34.7 32.6 32.6
```

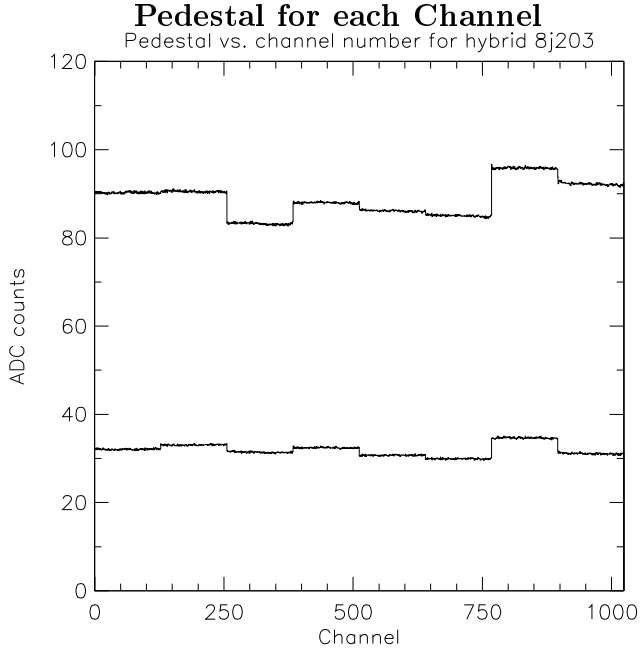
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

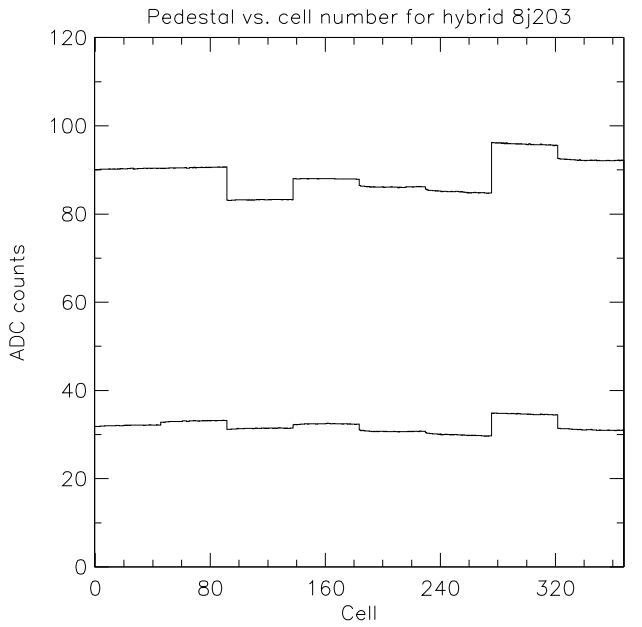
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

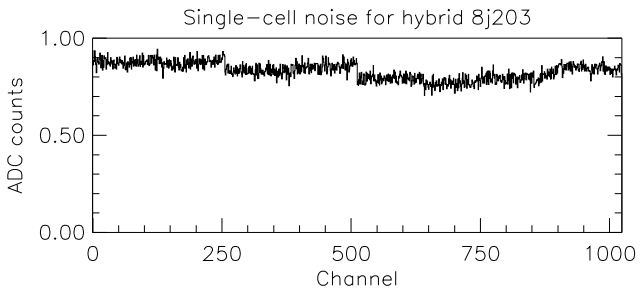
Pedestal vs. Pipeline Cell ID

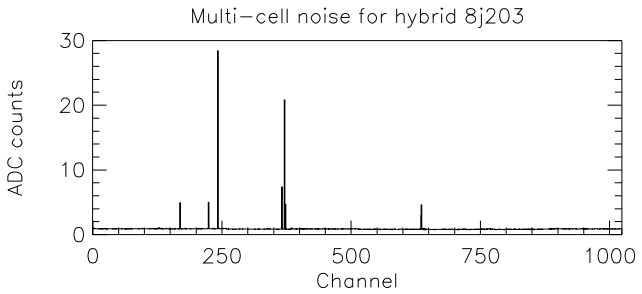


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

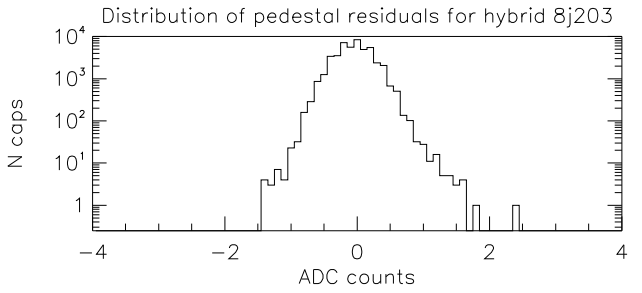
RMS Noise

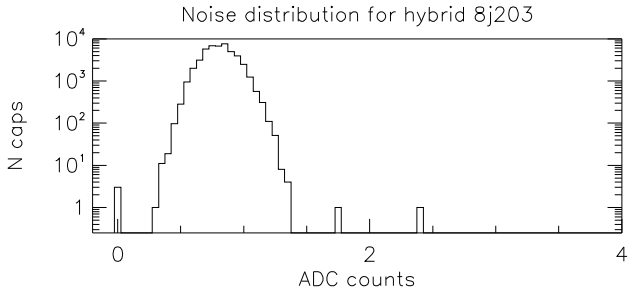




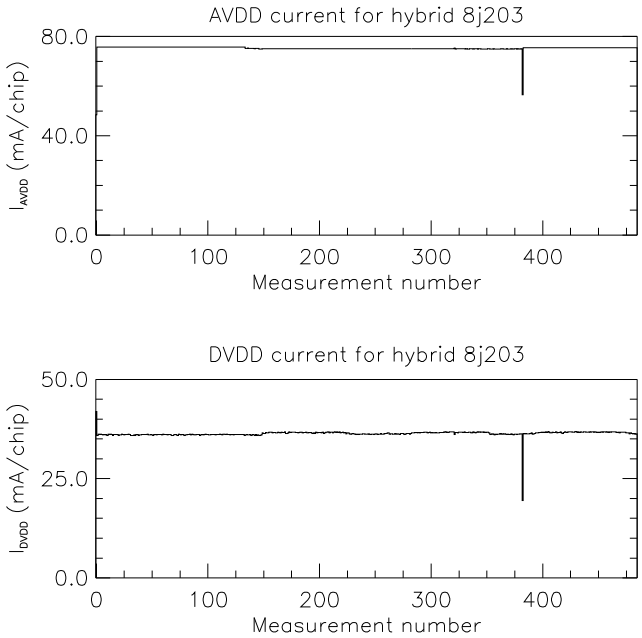
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in