Hybrid 8j205 Traveler

February 7, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J205 has die: 177-104 177-105 177-106 177-107 179-093 179-094 179-096 179-097

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

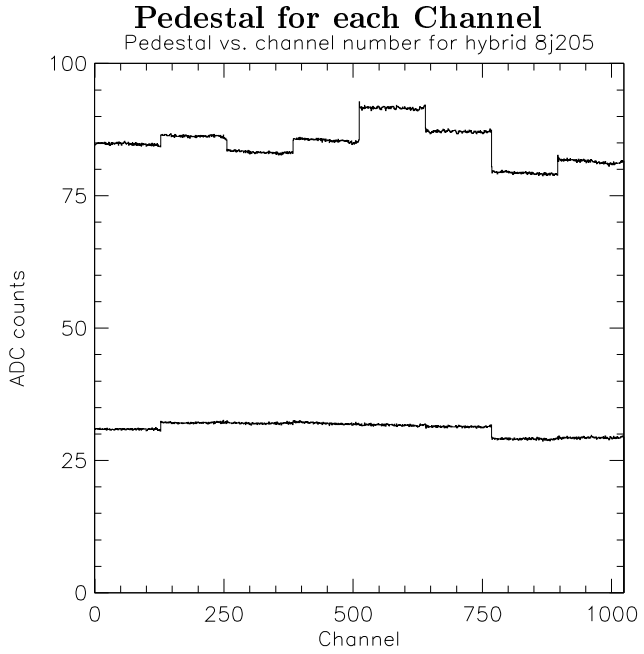
```
% Hybrid 8j205 classification info. Created 11:09:23 02/07/00

Hybrid 8j205 quality: fair
Chip classification: good good good good good good fair good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 6-42-101 6-42-102 6-43-96
   6-44-91 6-44-92
Channels at pedestal needed for DCMS: 34.2 34.7 35.7 34.6 32.7 33.7 36.6 35.6
```

4 Comments

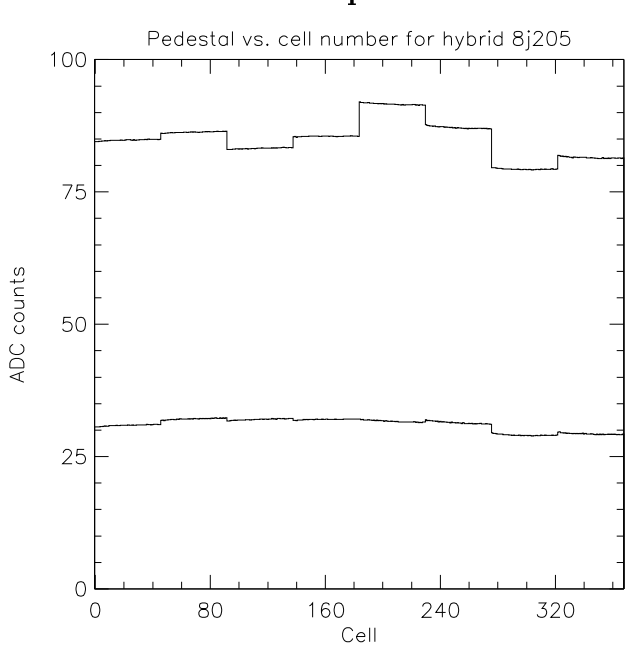
Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



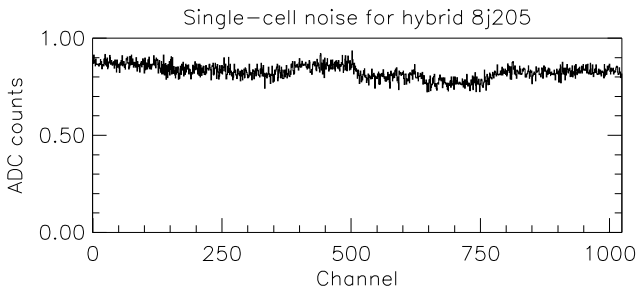
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

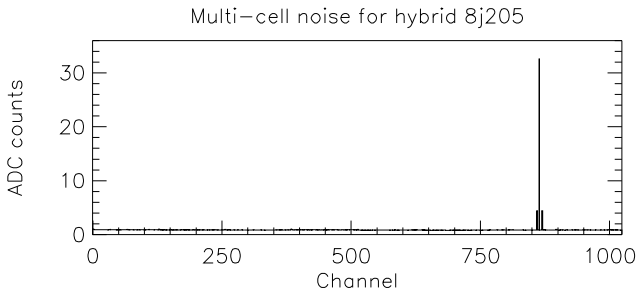


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

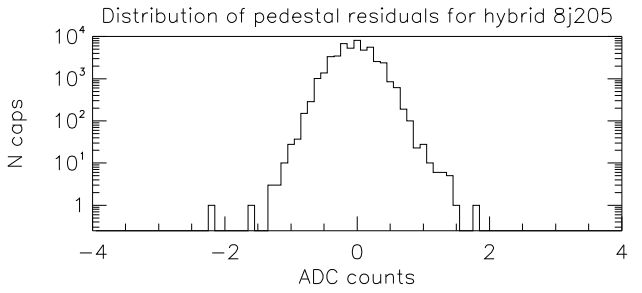
RMS Noise

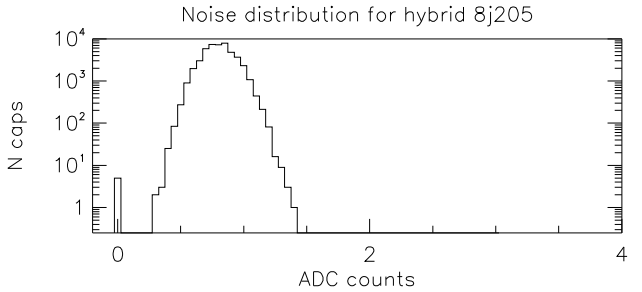




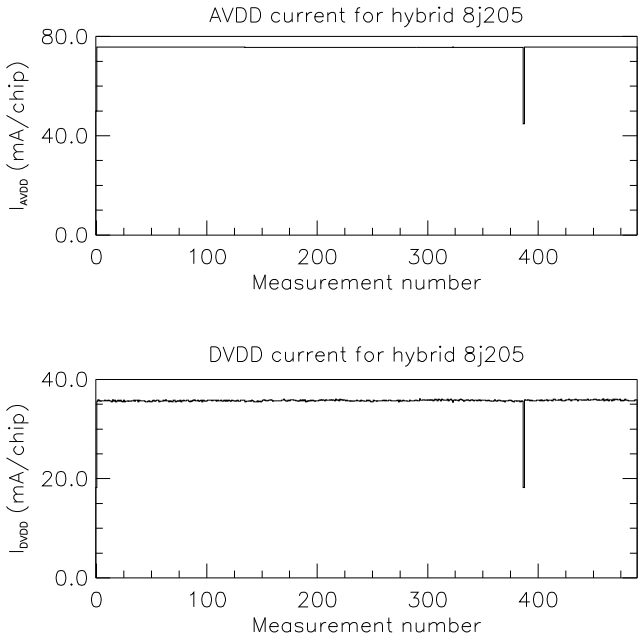
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in