Hybrid 8j25 Traveler

October 26, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J25 has die: 064-001 001-021 053-015 053-016 054-006 054-007 033-029 033-034

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid v3-025 classification info. Created 18:42:18 10/22/99

Hybrid v3-025 quality: fair
Chip classification: fair fair fair good good good fair good
Bad channels (chip-channel): 6-96
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-0-93 0-1-93 0-2-93 0-23-93 0-3-93 1-30-109 2-38-117 2-38-118 2-38-119 6-38-96
Channels at pedestal needed for DCMS: 34.7 34.6 34.6 34.8 33.6 33.6 36.3 36.6
```

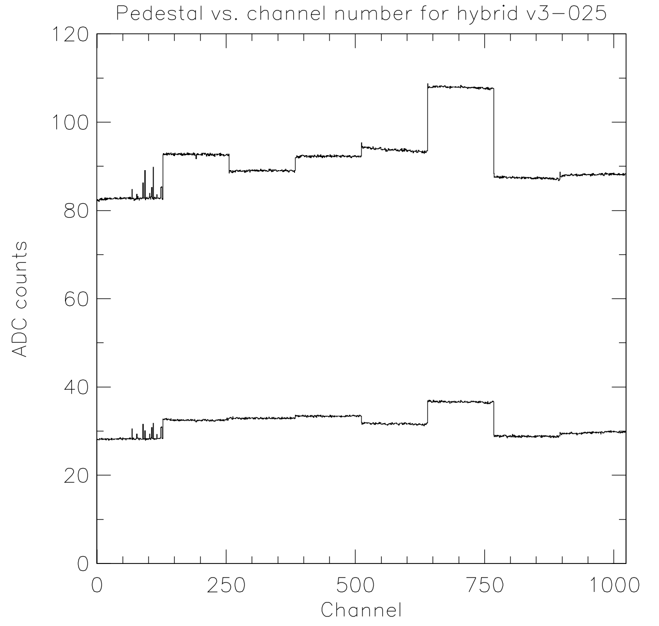
4 Comments

No comments.

5 Pedestal

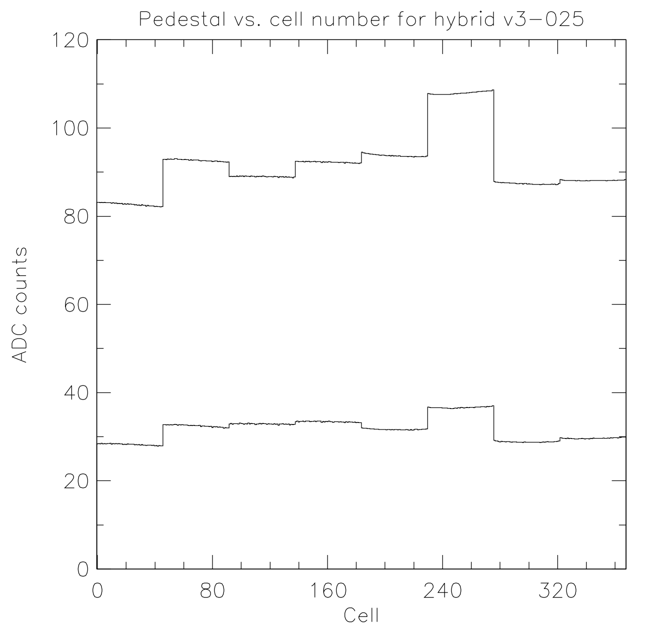
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

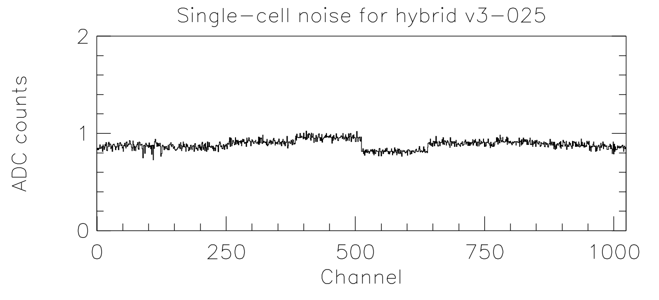
Pedestal vs. Pipeline Cell ID



6 Noise

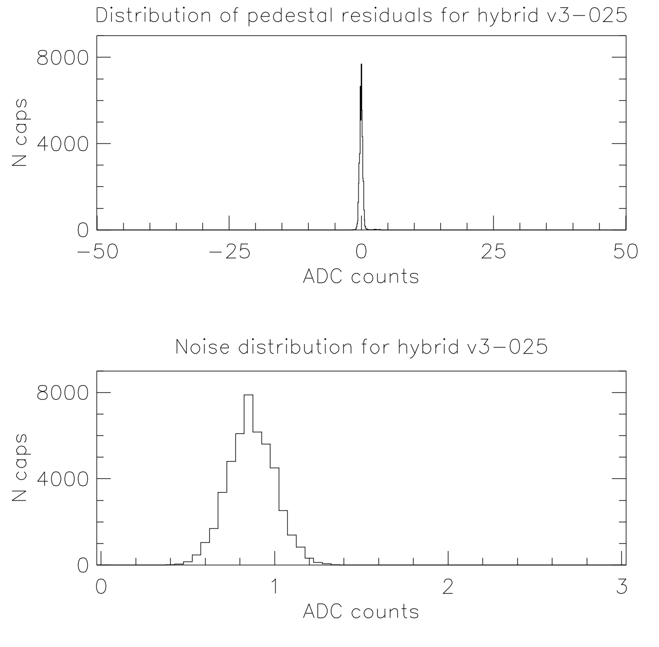
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in