Hybrid 8j273 Traveler

March 6, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J273 has die: 186-001 186-003 186-007 186-008 142-072 142-078 142-079 142-080

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j273 classification info. Created 10:32:27 03/06/00

Hybrid 8j273 quality: fair
Chip classification: good good good fair good fair fair good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-42-124 3-42-125 5-4-66
   5-4-67 5-5-67 6-18-5 6-35-5 6-38-5 6-40-5 6-42-5 6-5-4
   6-5-5
Channels at pedestal needed for DCMS: 31.6 30.7 32.5 32.6 33.5 29.6 31.7 33.7
```

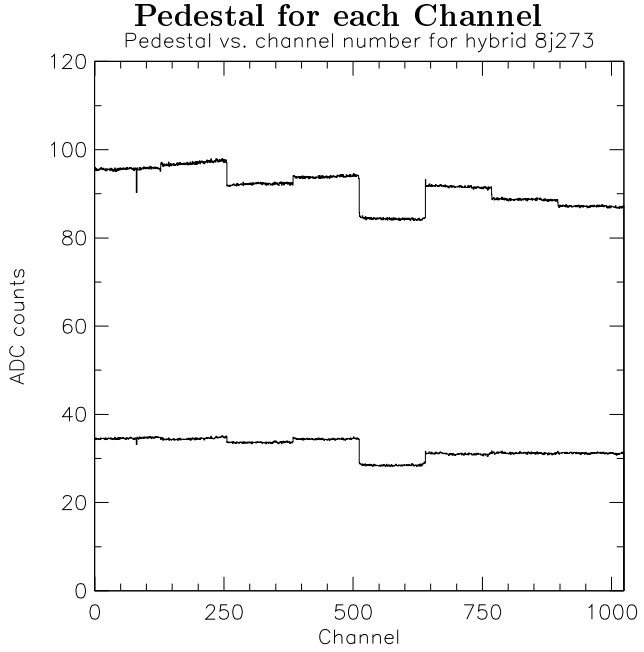
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

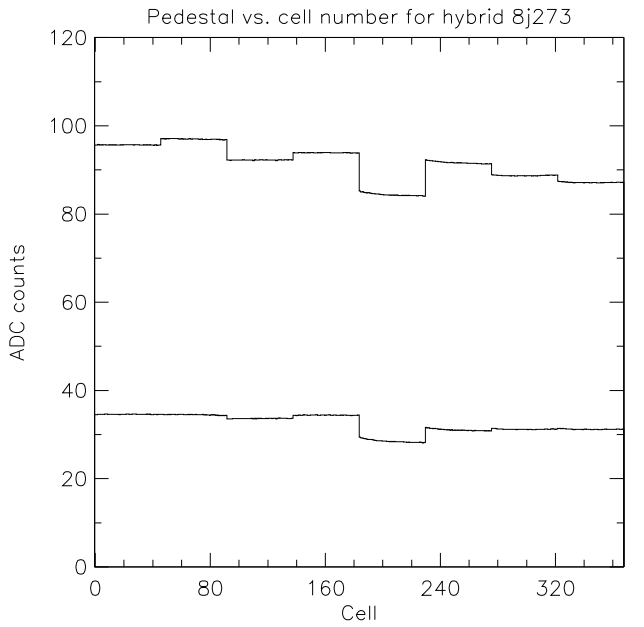
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

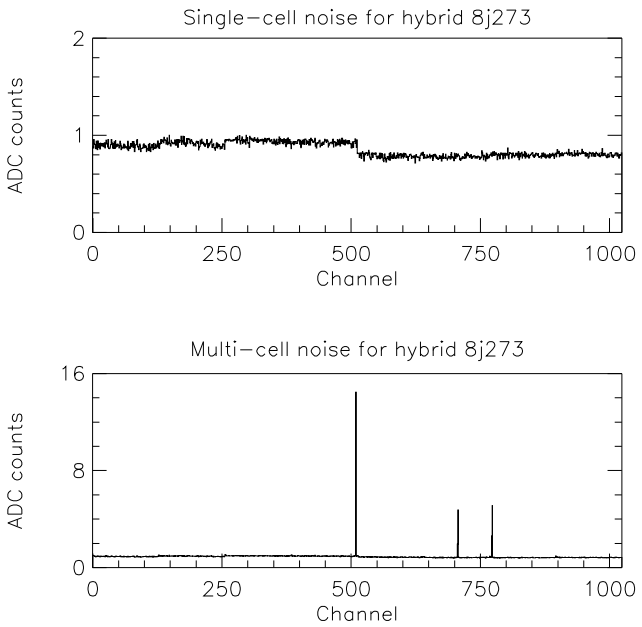
Pedestal vs. Pipeline Cell ID



6 Noise

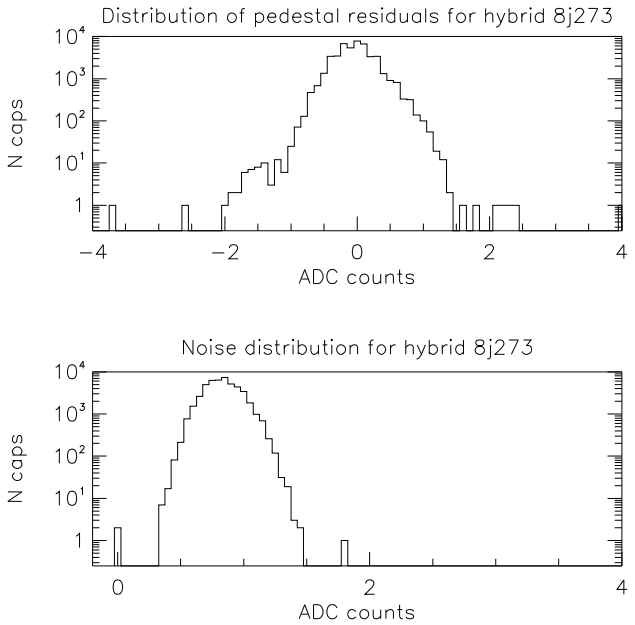
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise

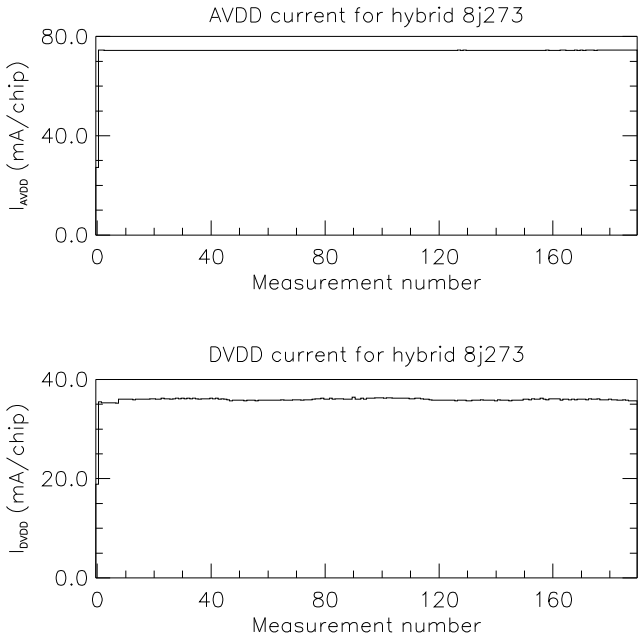


The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in