Hybrid 8j285 Traveler

March 1, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J285 has die: 163-012 163-014 163-015 163-017 141-030 141-031 141-032 141-035

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j285 classification info. Created 10:50:14 03/01/00

Hybrid 8j285 quality: fair
Chip classification: fair good fair good good good good good
Bad channels (chip-channel): 0-99 2-21
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-22-100 0-22-101 0-23-101
   0-26-100 0-26-101 0-27-101 0-29-100 0-29-101 0-31-100 0-31-101 0-33-100
   0-33-101 0-42-100 0-42-101 0-43-101 0-9-101
Channels at pedestal needed for DCMS: 33.1 33.2 32.6 31.6 31.7 30.7 29.8 31.6
```

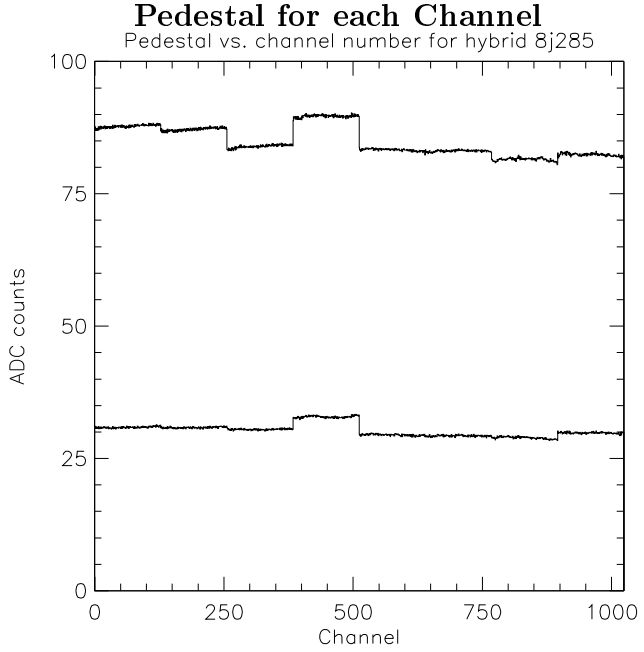
4 Comments

Encapsulated. FE DV finger gold bonds. HV tested.

5 Pedestal

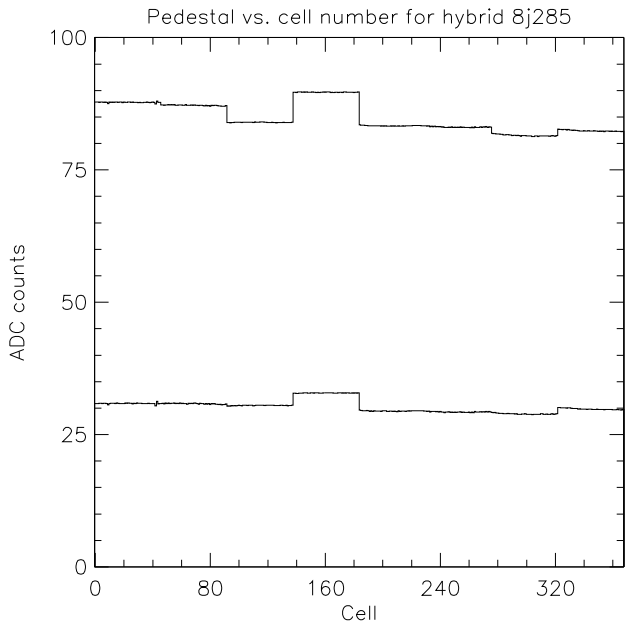
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

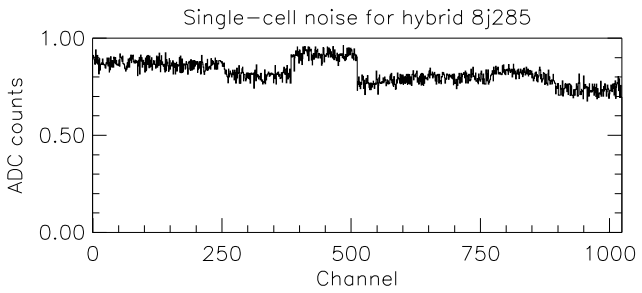
Pedestal vs. Pipeline Cell ID

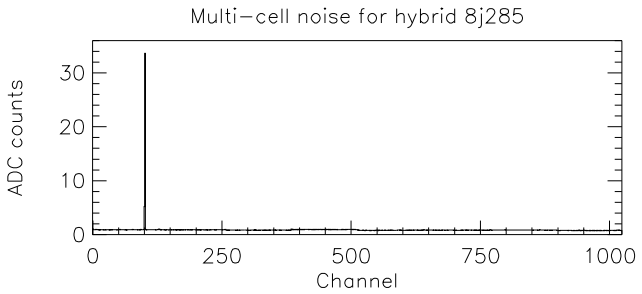


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

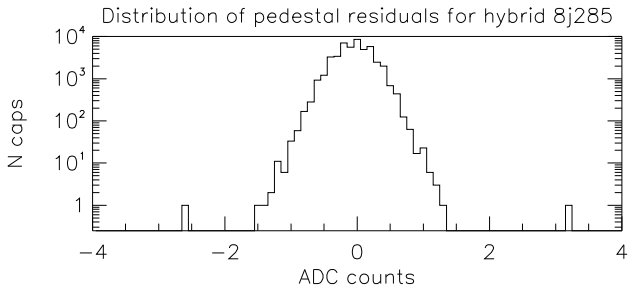
RMS Noise

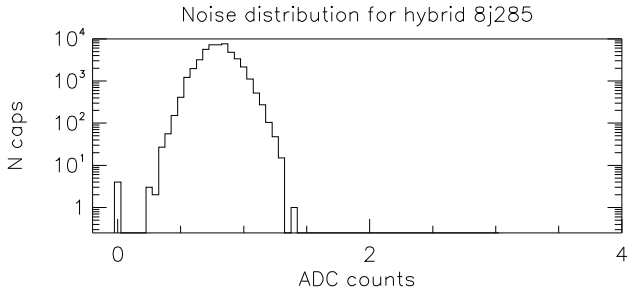




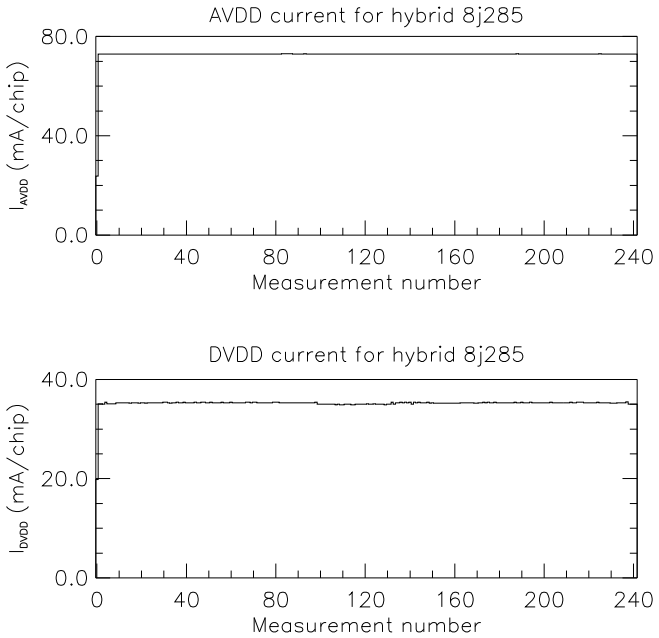
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in