# Hybrid 8j3 Traveler

October 29, 1999

## 1 Connectivity

Repairs on shorts:

Fixes for opens:

## 2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J3 has die: 088-031 088-032 088-038 088-048 001-037 001-038 001-039 001-040

## 3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j3 classification info. Created 11:17:16 10/29/99

Hybrid 8j3 quality: fair
Chip classification: good good good fair fair fair fair fair
Bad channels (chip-channel): 3-21 4-74 5-55 5-56 6-39 7-127
Bad cells: none
Random bad capacitors (chip-cell-channel): 5-39-80 6-45-39 7-3-127
Channels at pedestal needed for DCMS: 34.5 33.6 33.6 33.7 34.6 34.5 34.6 36.6
```

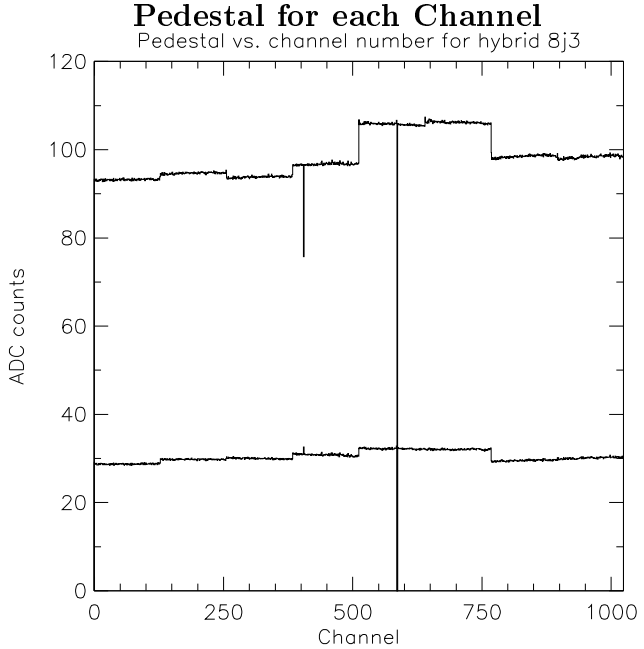
## 4 Comments

No comments.

# 5 Pedestal

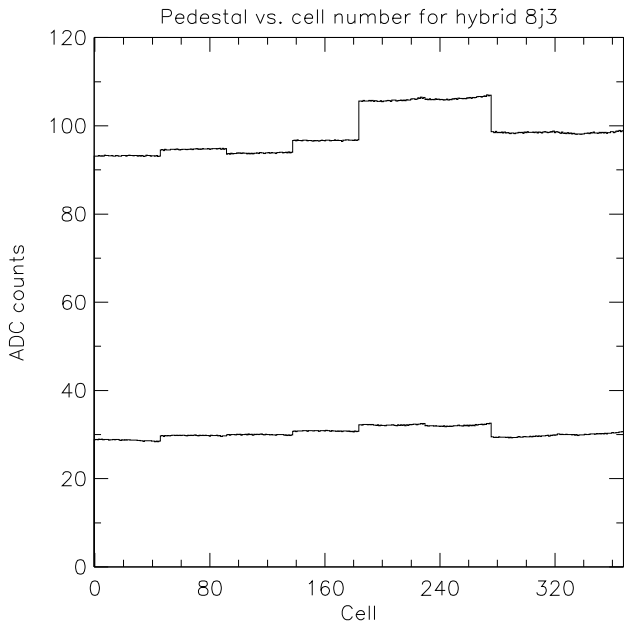
The following plot shows the pedestals vs. channel number with and without charge injection:

**Pedestal for each Channel**




The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

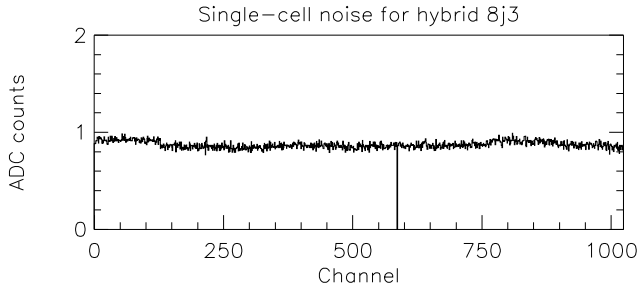
**Pedestal vs. Pipeline Cell ID**

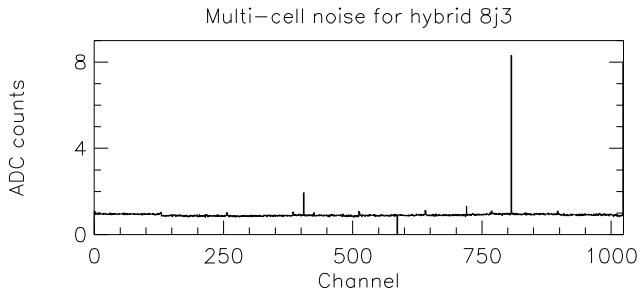


# 6 Noise

The following plots show the single-cell and multi-cell RMS noise:

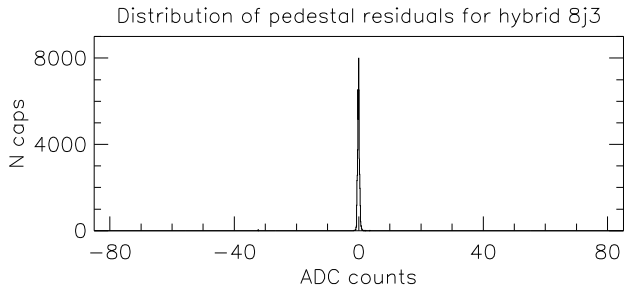
**RMS Noise**

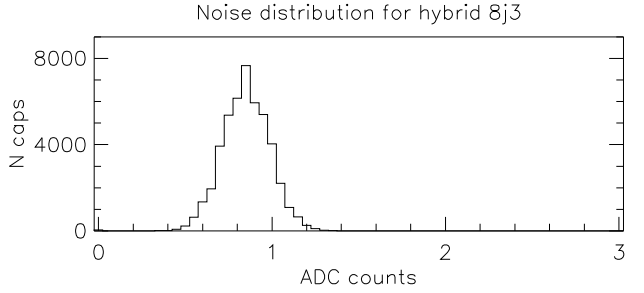


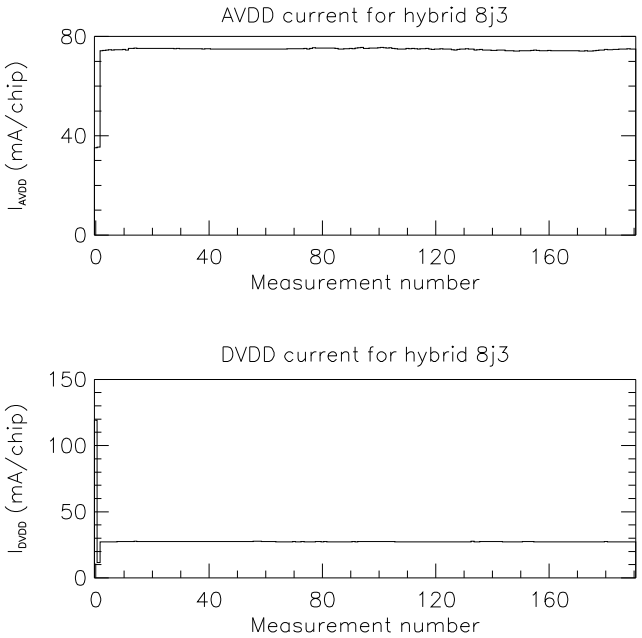

The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

**Distribution of Pedestals and Noise**



# 7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

**Supply Currents During Burn-in**