Hybrid 8j30 Traveler

March 30, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J30 has die: 045-051 050-002 050-003 050-005 045-010 045-011 045-012 045-013

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

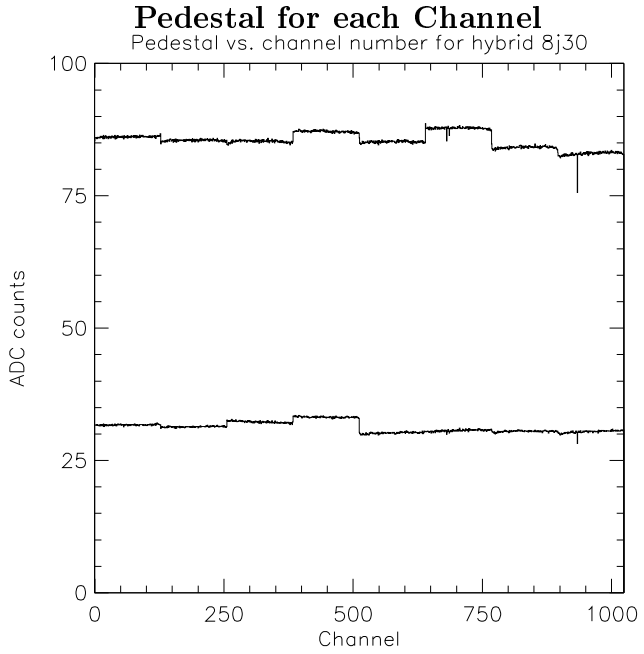
```
% Hybrid 8j30 classification info. Created 08:45:48 03/24/00

Hybrid 8j30 quality: fair
Chip classification: fair good good good good good good fair
Bad channels (chip-channel): 7-38
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-10-89 0-14-57 7-0-62
Channels at pedestal needed for DCMS: 33.6 33.6 33.7 33.7 33.7 33.6 32.6 33.9
```

4 Comments

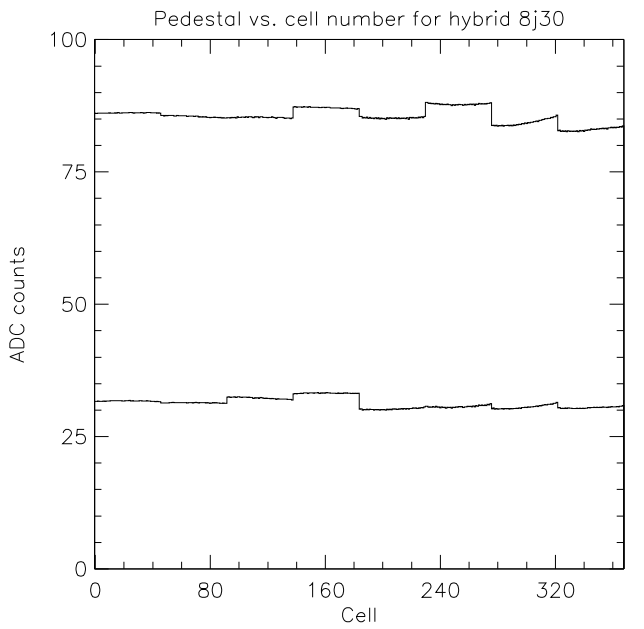
HV tested.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



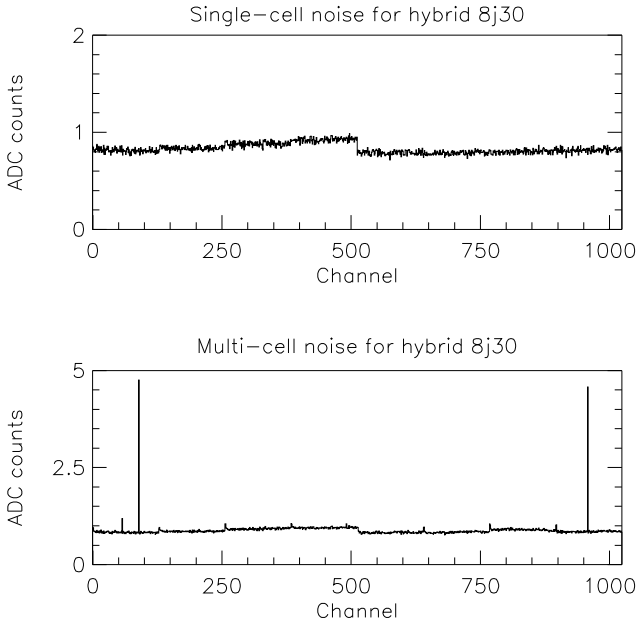
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.



6 Noise

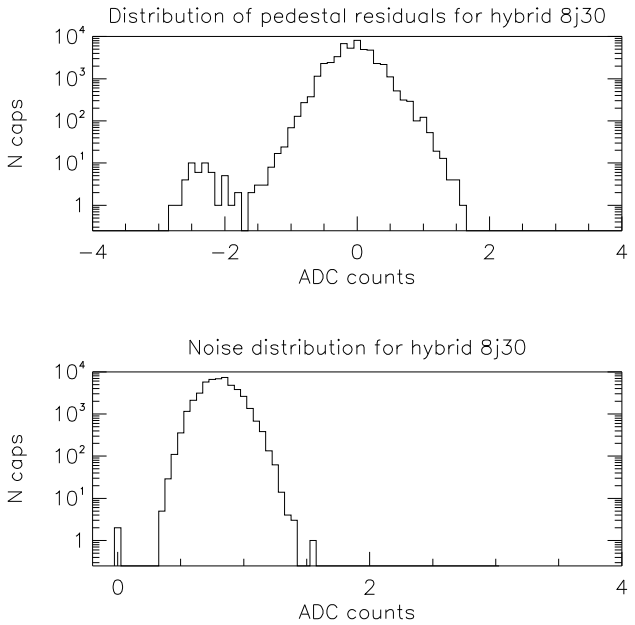
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise

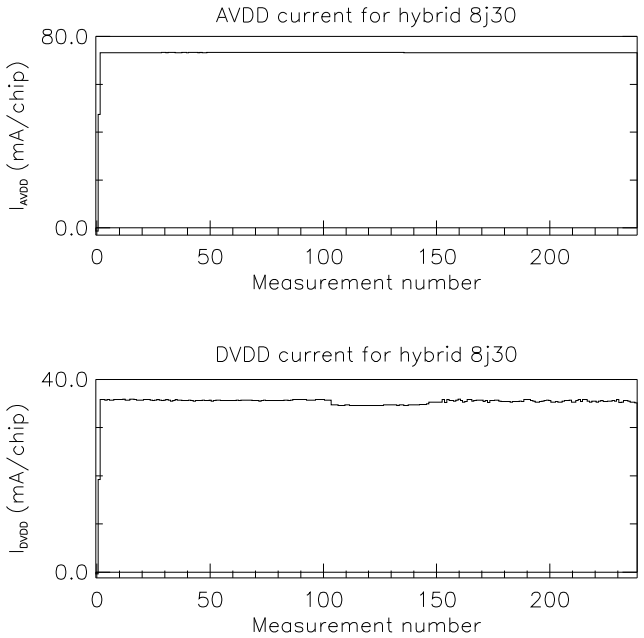


The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in