Hybrid 8j324 Traveler

May 8, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J324 has die: 206-002 206-008 206-009 206-011 154-058 154-059 154-063 154-064

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j324 classification info. Created 09:49:17 05/08/00

Hybrid 8j324 quality: bad
Chip classification: fair good bad fair fair good good fair
Bad channels (chip-channel): 0-127 2-18 2-27 2-40 2-46 4-45
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-11-46 2-20-46 2-22-46
   2-33-46 2-39-46 2-42-46 2-44-46 2-9-46 3-41-75 4-38-2 7-33-89
Channels at pedestal needed for DCMS: 33.7 32.7 31.6 33.6 33.6 30.7 32.6 33.7
```

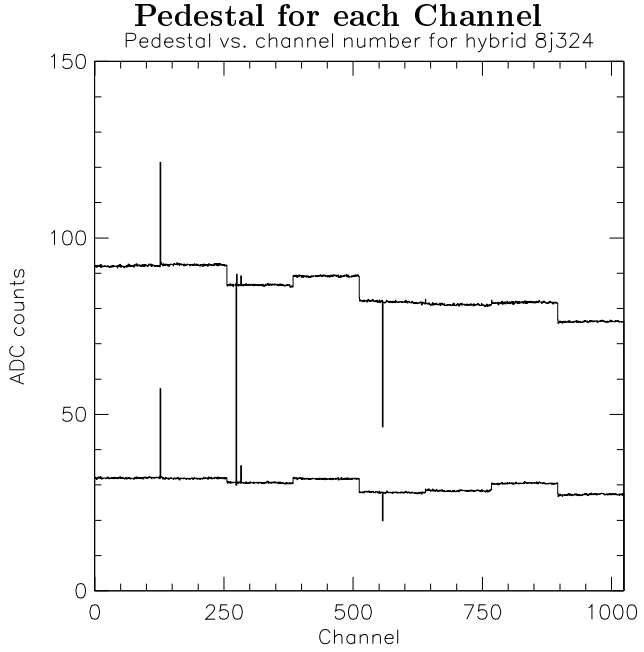
4 Comments

HV tested.

5 Pedestal

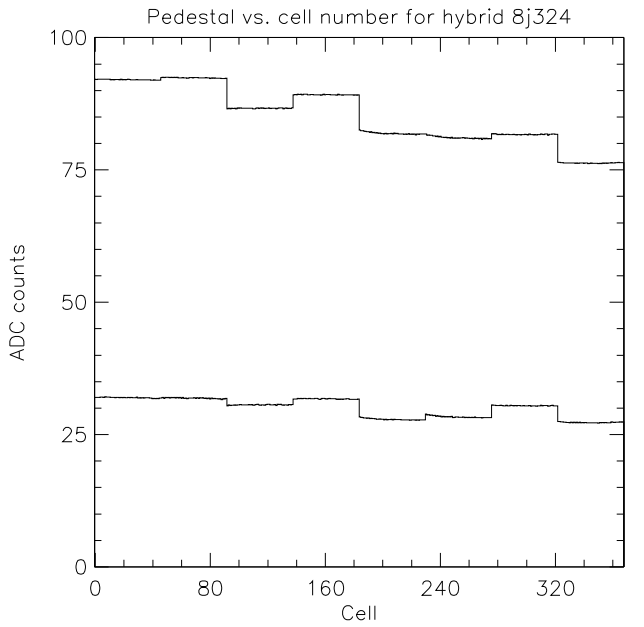
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

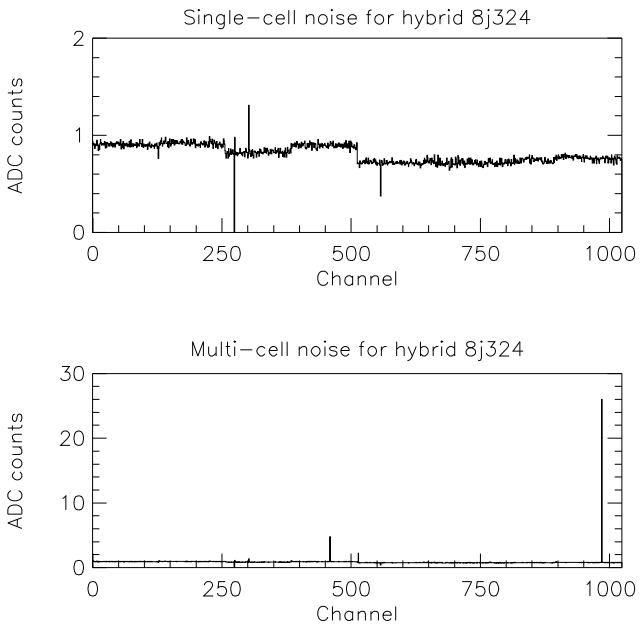
Pedestal vs. Pipeline Cell ID



6 Noise

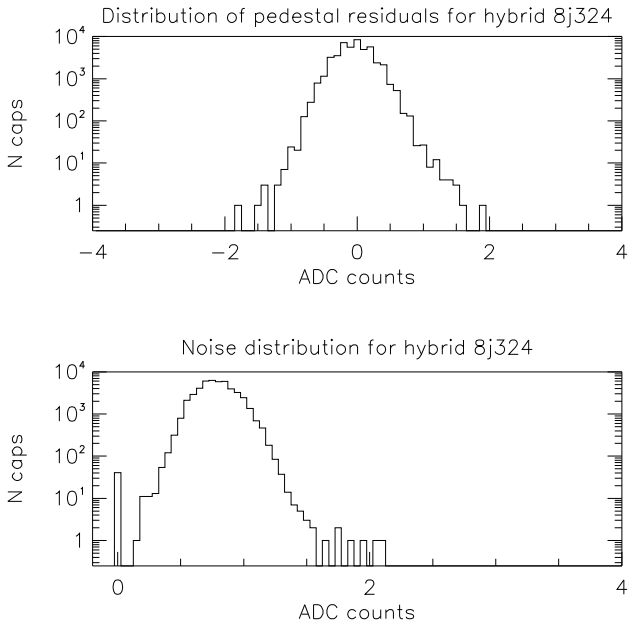
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise

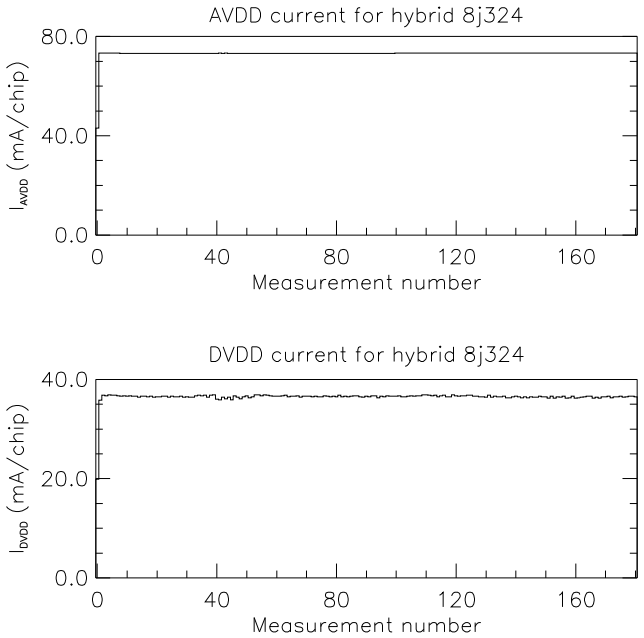


The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in