Hybrid 8j326 Traveler

May 4, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J326 has die: 206-016 206-018 206-021 206-022 154-081 154-082 154-085 154-086

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j326 classification info. Created 11:15:33 05/03/00

Hybrid 8j326 quality: fair
Chip classification: fair good fair fair good fair good good
Bad channels (chip-channel): 0-63 2-41 5-106
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-25-58 0-43-105 0-9-90
   3-23-53
Channels at pedestal needed for DCMS: 30.7 31.6 30.7 31.7 34.2 34.5 33.7 32.7
```

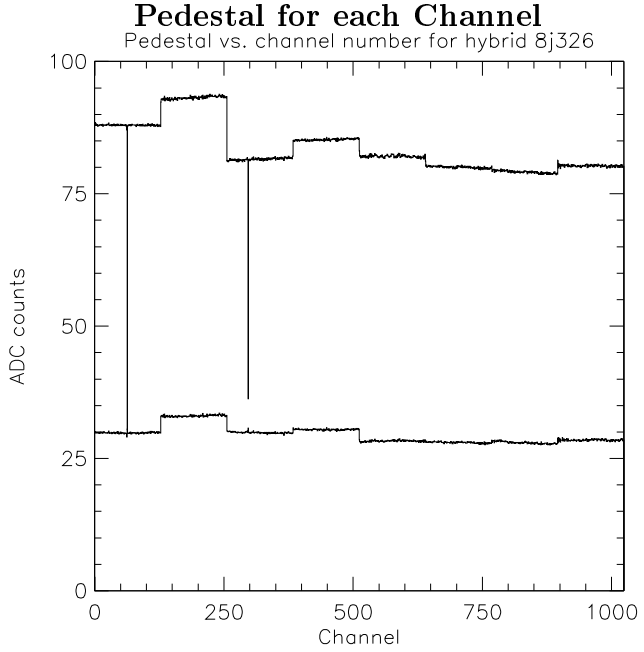
4 Comments

HV tested.

5 Pedestal

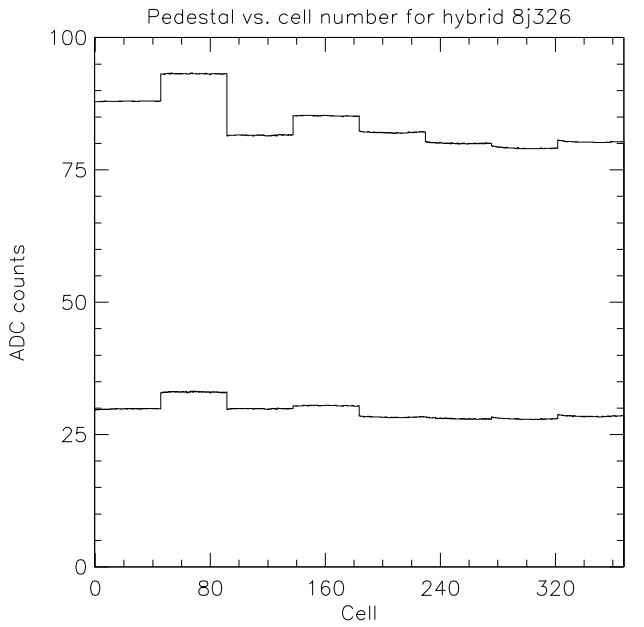
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

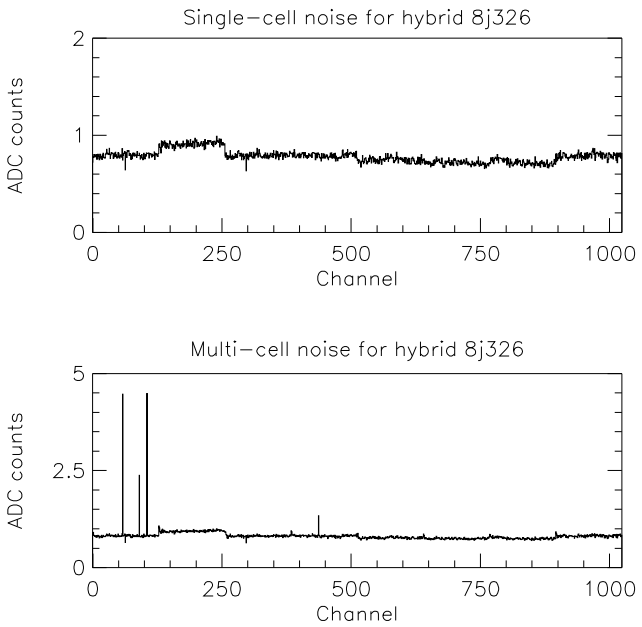
Pedestal vs. Pipeline Cell ID



6 Noise

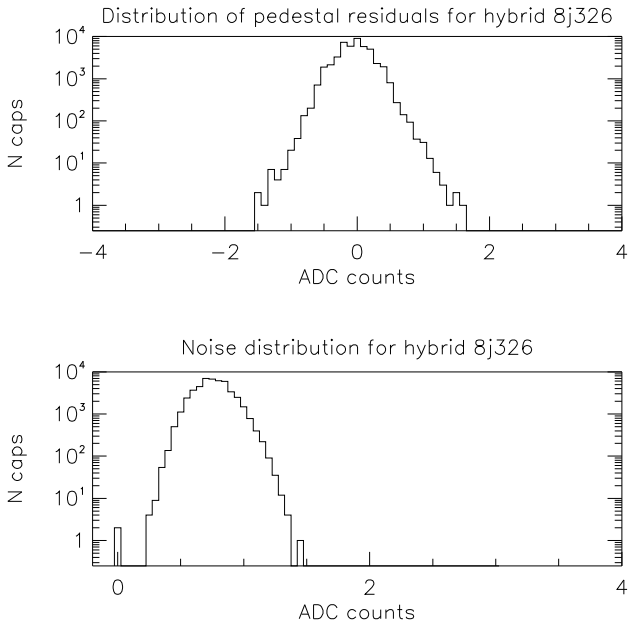
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise

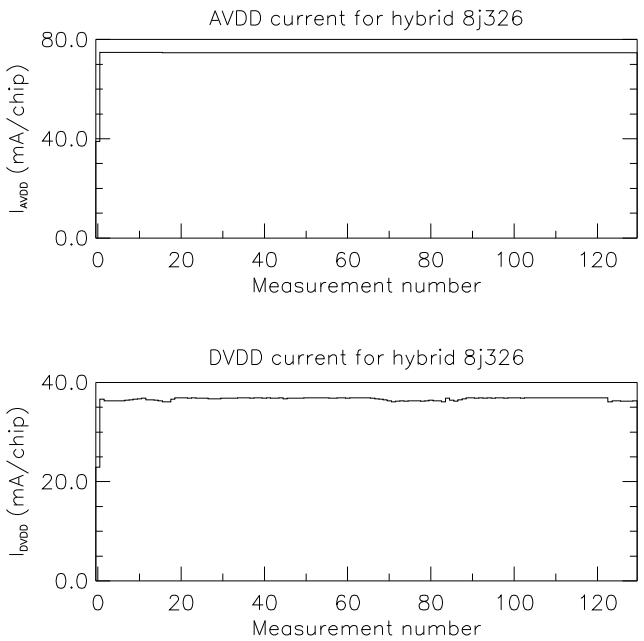


The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in