Hybrid 8j358 Traveler

May 26, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J358 has die: 236-130 236-131 206-040 206-043 236-102 236-103 236-104 236-106

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j358 classification info. Created 11:20:54 05/24/00

Hybrid 8j358 quality: fair
Chip classification: fair fair fair fair good good good good
Bad channels (chip-channel): 0-66 2-45
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-24-31 0-24-32 0-24-33
   0-28-44 0-28-45 0-29-6 0-29-7 1-21-53 3-0-106 3-0-107 3-25-106
   3-25-107 3-26-107 3-29-106 3-29-107 3-32-106 3-32-107 3-34-106 3-34-107
   3-35-92 3-35-93 3-36-106 3-36-107 3-45-106 3-45-107
Channels at pedestal needed for DCMS: 31.4 30.6 29.7 28.9 32.2 32.6 30.6 32.6
```

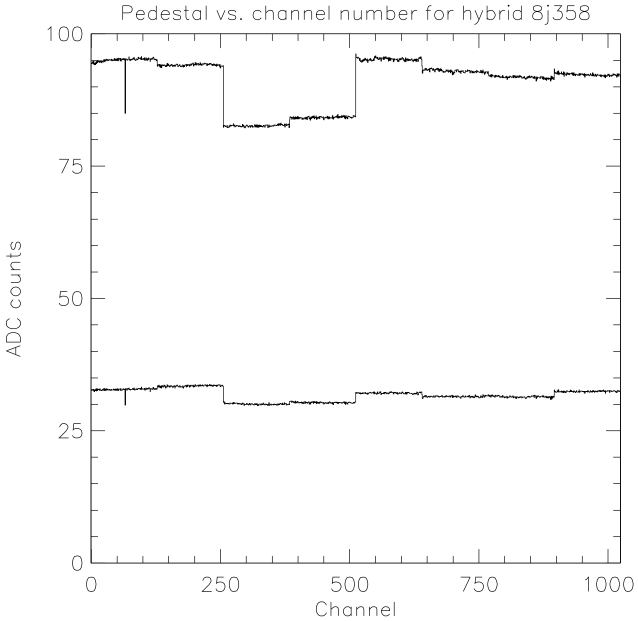
4 Comments

HV tested.

5 Pedestal

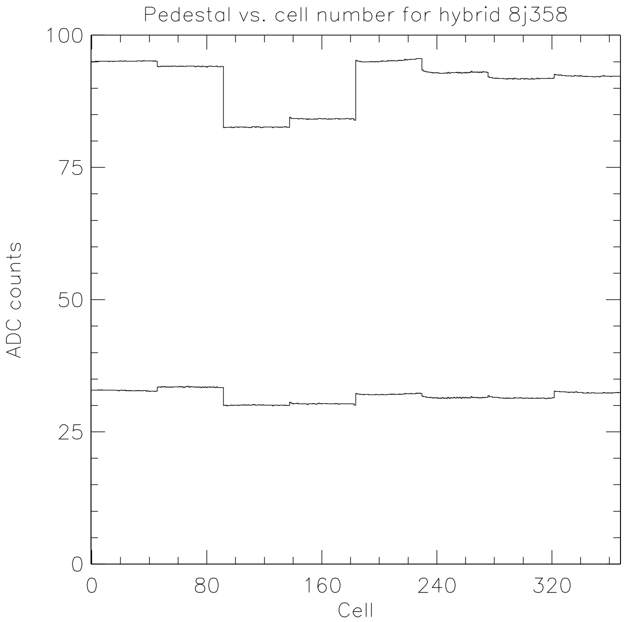
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

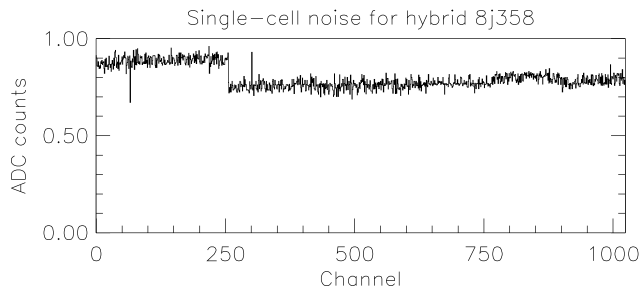
Pedestal vs. Pipeline Cell ID

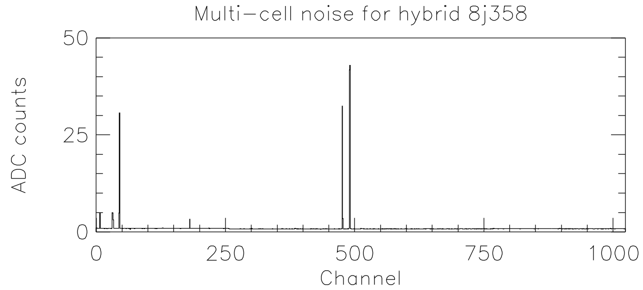


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

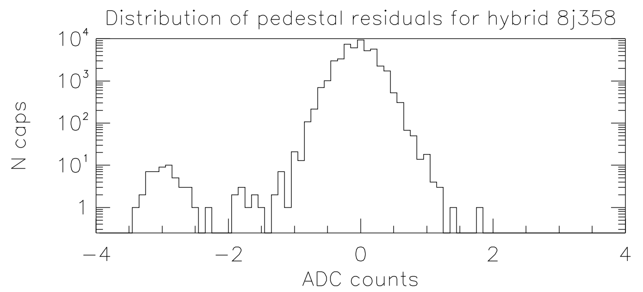
RMS Noise

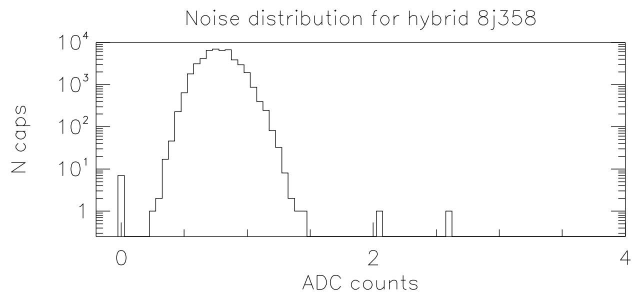




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in