Hybrid 8j362 Traveler

June 26, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J362 has die: 168-104 168-105 168-106 168-107 206-073 206-075 206-076 206-077

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j362 classification info. Created 13:38:40 06/21/00

Hybrid 8j362 quality: fair
Chip classification: fair fair good good good fair good good
Bad channels (chip-channel): 1-84
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-21-15 0-21-16 0-34-14
   0-34-15 0-34-16 0-34-17 0-38-14 0-38-15 0-38-16 0-38-17 0-39-15
   0-39-16 0-41-14 0-41-15 0-41-16 0-41-17 0-43-14 0-43-15 0-43-16
   0-43-17 0-45-14 0-45-15 0-45-16 0-45-17 0-8-14 0-8-15 0-8-16
   0-8-17 0-9-15 0-9-16 5-0-114 5-0-115 5-1-115 5-30-115 5-35-115
Channels at pedestal needed for DCMS: 32.7 32.6 31.3 31.6 30.6 32.2 31.7 31.7
```

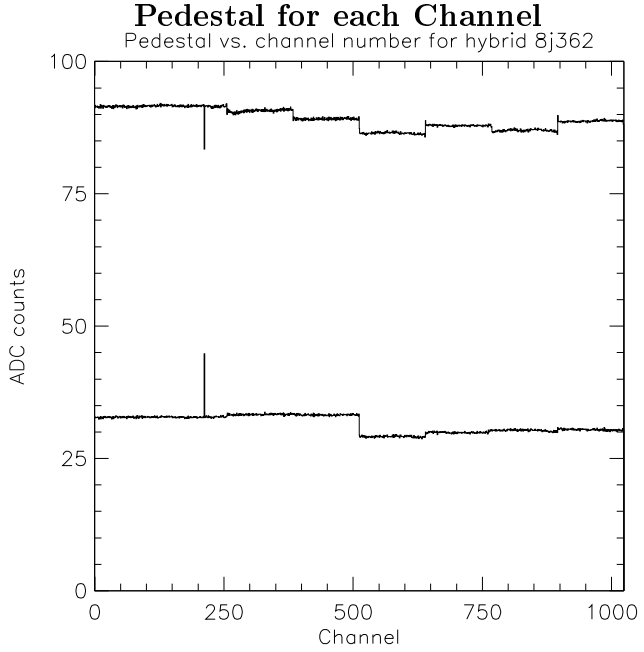
4 Comments

HV tested.

5 Pedestal

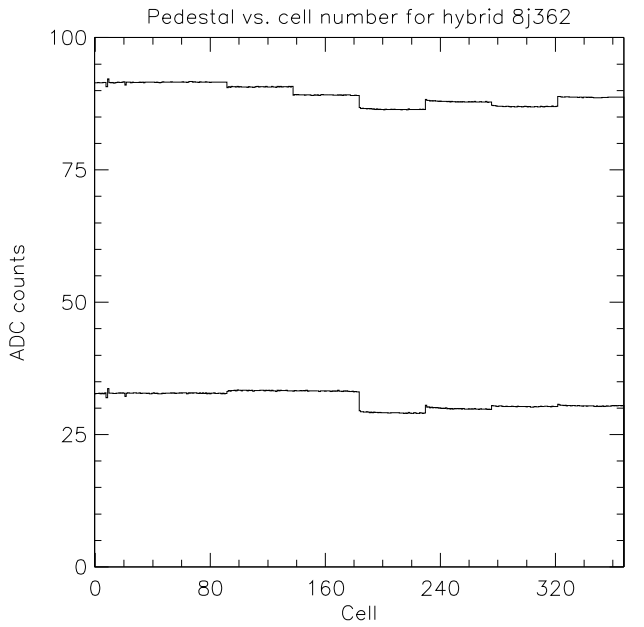
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

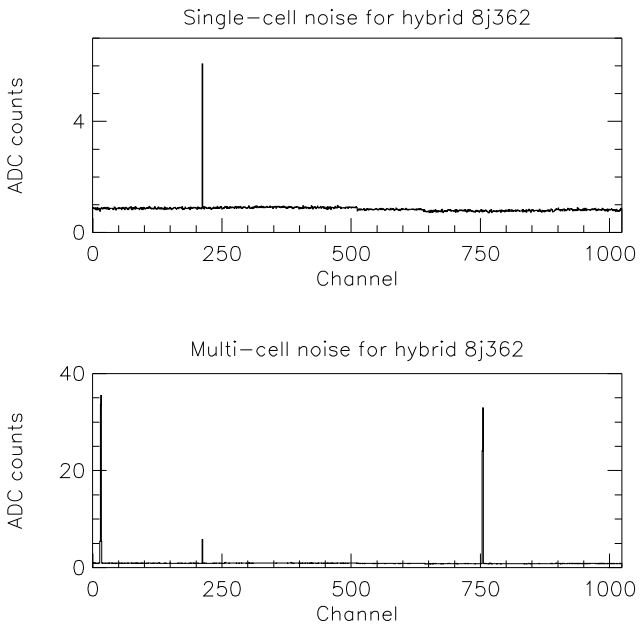
Pedestal vs. Pipeline Cell ID



6 Noise

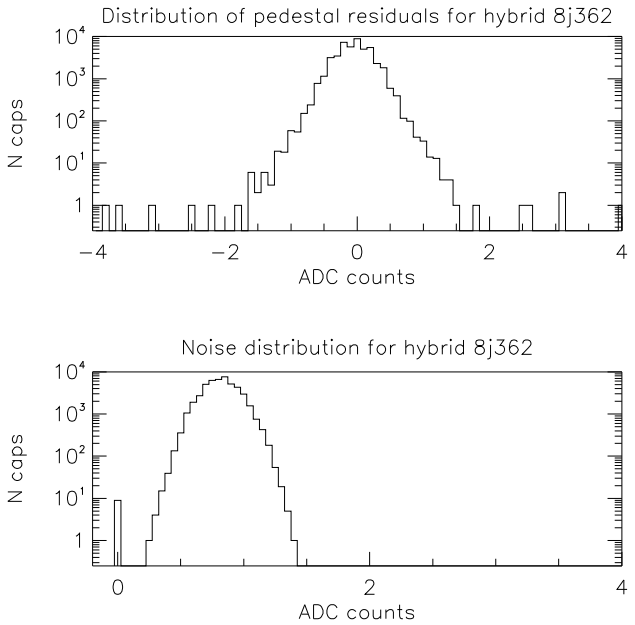
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise

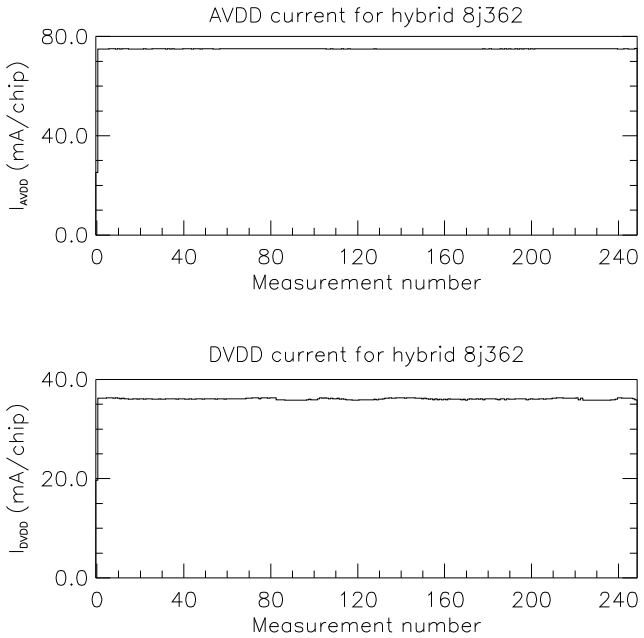


The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in