Hybrid 8j4 Traveler

June 5, 2000

1 Connectivity

Repairs on shorts:
Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J4 has die: 088-052 001-041 001-042 234-084 001-044 001-045 001-046 001-047

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j4 classification info. Created 10:22:05 11/29/99

Hybrid 8j4 quality: fair
Chip classification: good fair fair fair fair good fair fair
Bad channels (chip-channel): 2-101 3-75 3-113 4-66 6-67 7-108
Bad cells: none
Random bad capacitors (chip-cell-channel): 1-39-117 2-33-127 7-31-108
Channels at pedestal needed for DCMS: 33.6 34.6 35.7 34.4 35.3 35.6 34.6 35.6
```

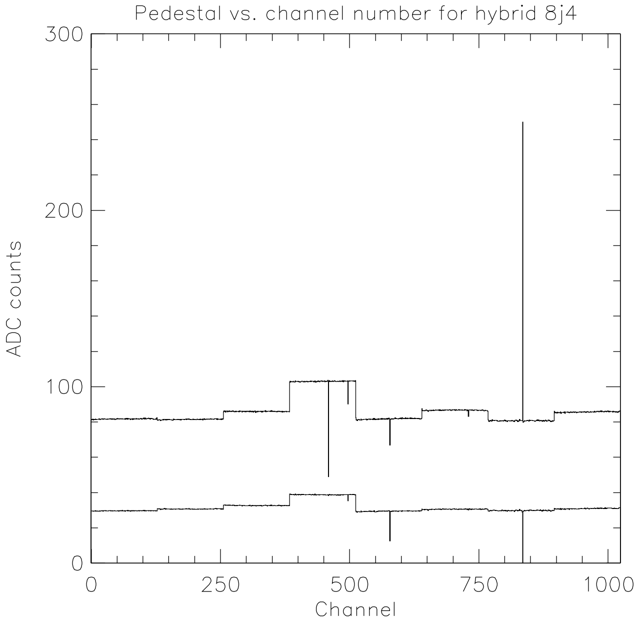
4 Comments

No comments.

5 Pedestal

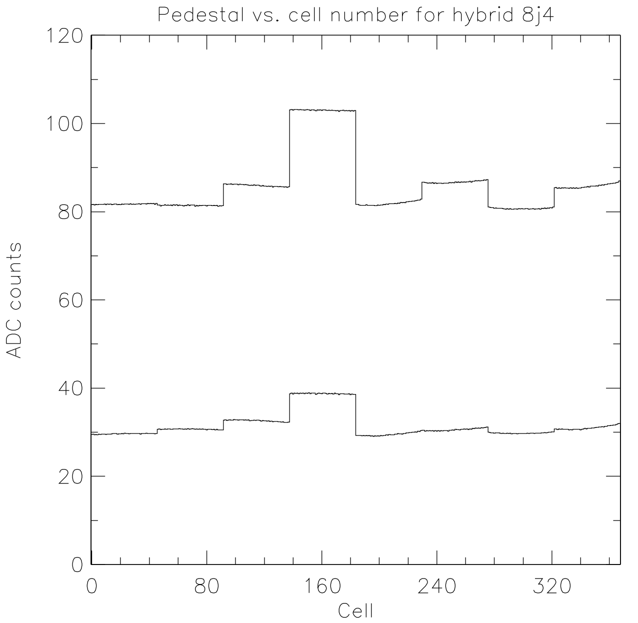
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

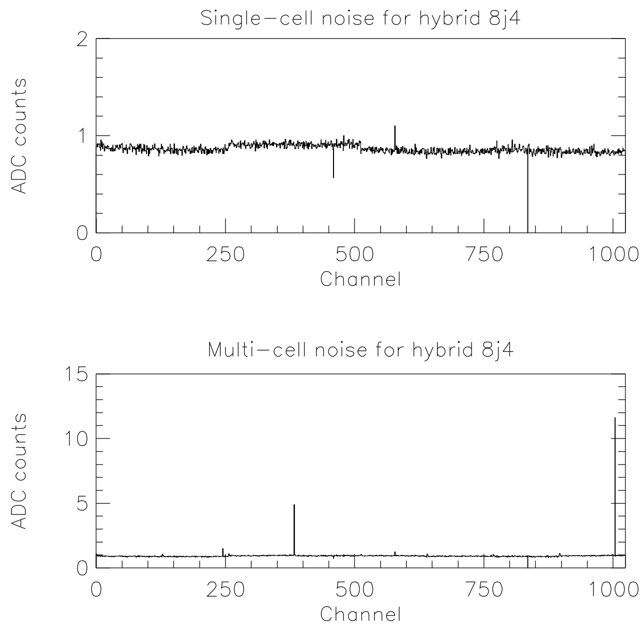
Pedestal vs. Pipeline Cell ID



6 Noise

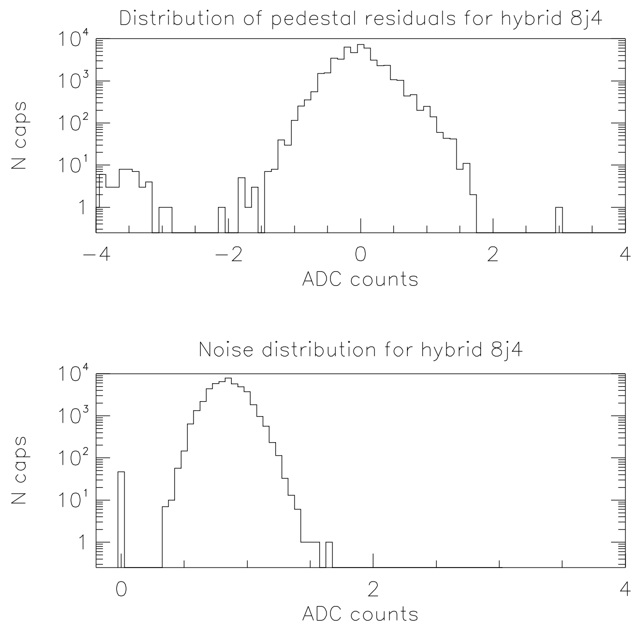
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in