Hybrid 8j53 Traveler

November 2, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J53 has die: 048-036 048-040 048-041 048-043 051-007 051-010 051-011 051-012

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j53 classification info. Created 18:52:45 10/27/99

Hybrid 8j53 quality: bad
Chip classification: good good good good good good fair bad
Bad channels (chip-channel): 6-72 6-114 7-78 7-80 7-81 7-82
Bad cells: none
Random bad capacitors (chip-cell-channel): 6-42-114 6-44-114 6-45-114 6-45-122
Channels at pedestal needed for DCMS: 34.1 34.6 34.6 33.6 33.1 33.6 33.6 32.6
```

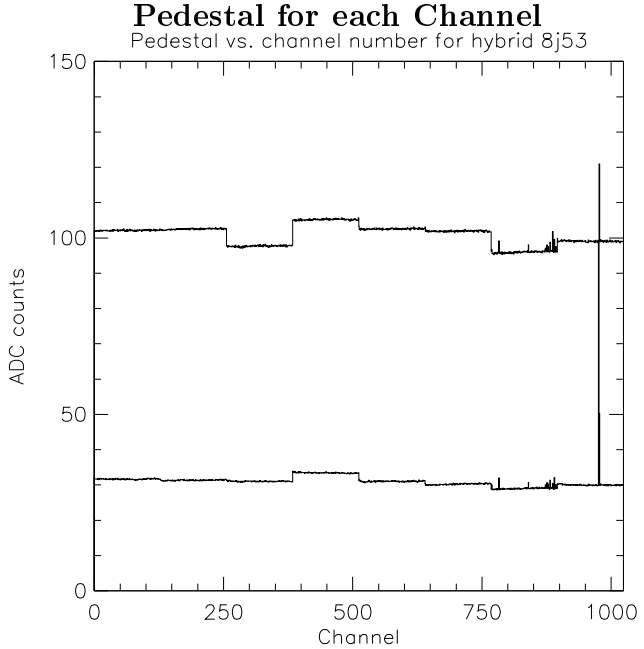
4 Comments

No comments.

5 Pedestal

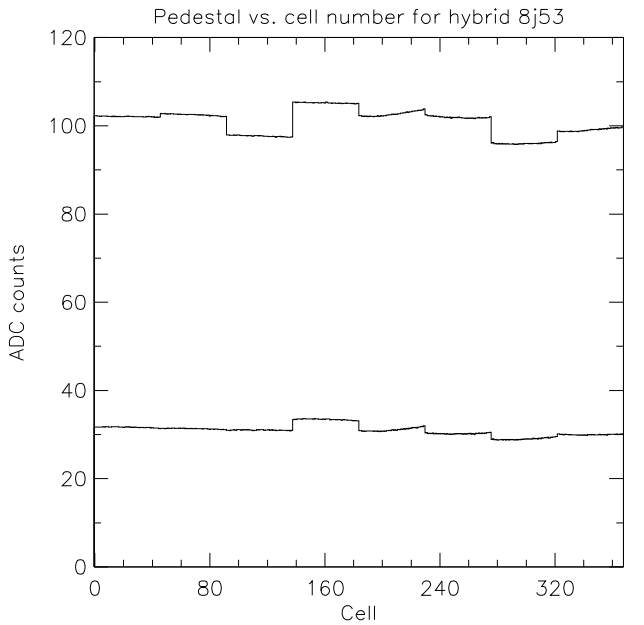
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

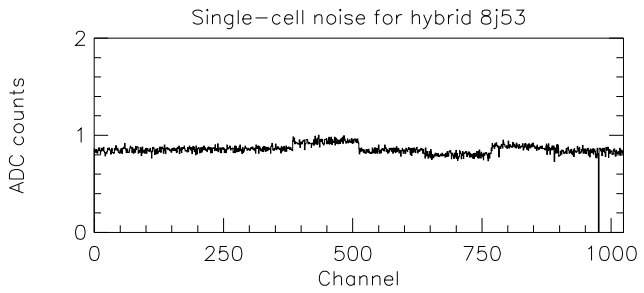
Pedestal vs. Pipeline Cell ID

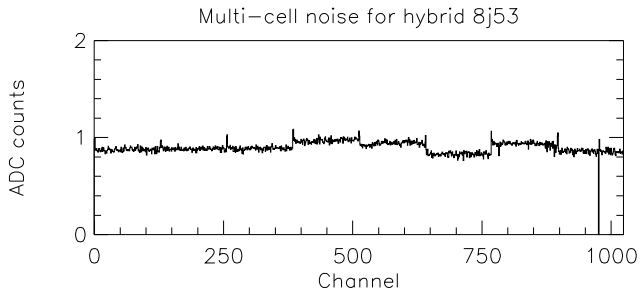


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

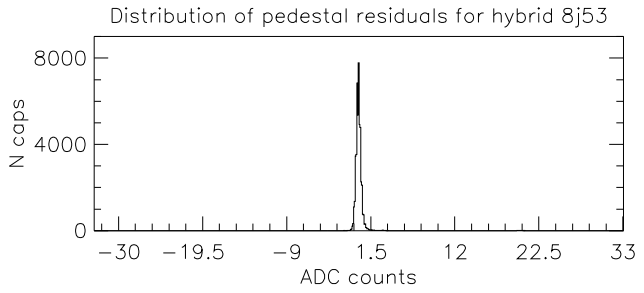
RMS Noise

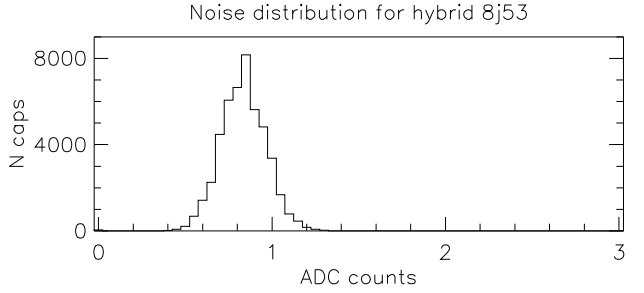




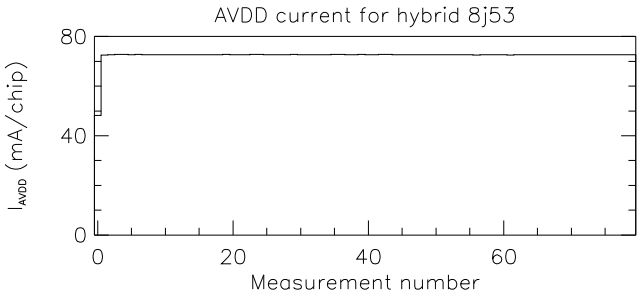
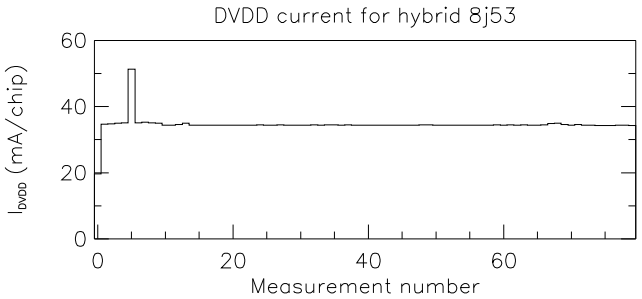
The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in