Hybrid 8j55 Traveler

November 8, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J55 has die: 051-024 051-025 051-026 051-030 068-023 068-024 068-025 068-026

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j55 classification info. Created 15:15:39 11/01/99

Hybrid 8j55 quality: bad
Chip classification: bad fair good good good good bad good
Bad channels (chip-channel): 0-0 0-62 0-86 0-104 1-0 6-42 6-43 6-44 6-45
Bad cells: none
Random bad capacitors (chip-cell-channel): 6-33-42
Channels at pedestal needed for DCMS: 34.3 35.2 33.7 33.6 33.4 33.7 32.6 34.4
```

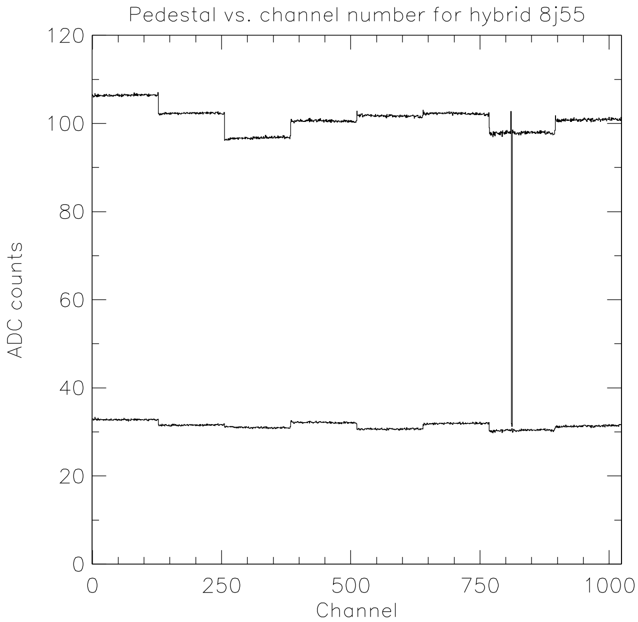
4 Comments

No comments.

5 Pedestal

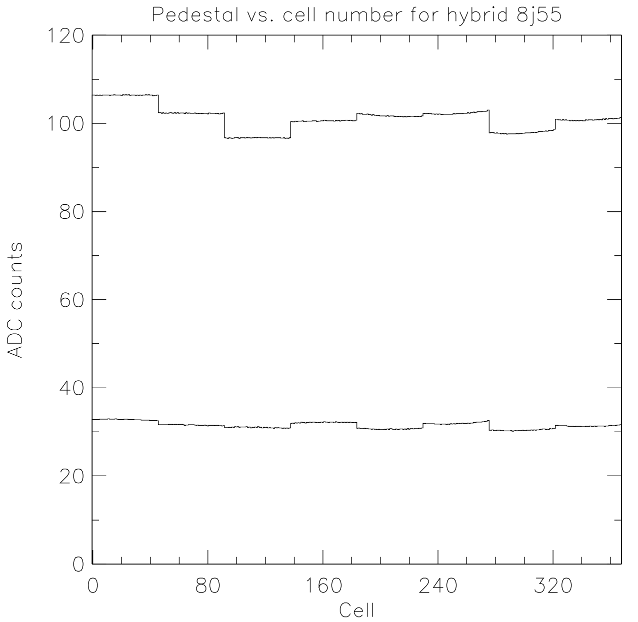
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

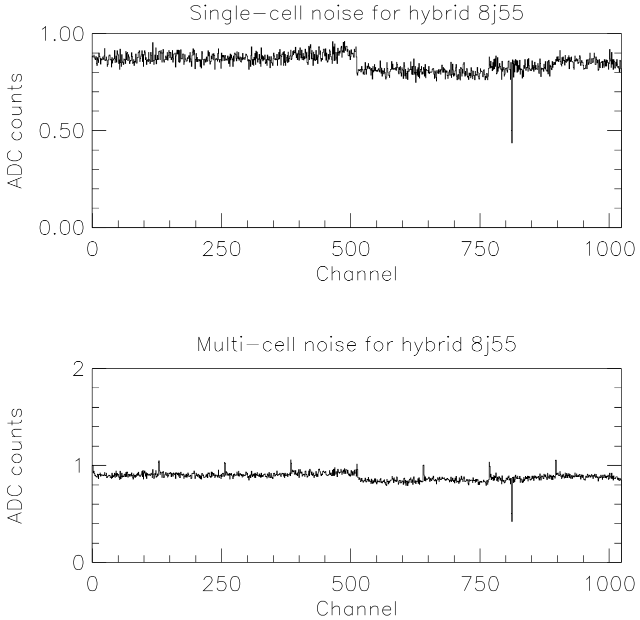
Pedestal vs. Pipeline Cell ID



6 Noise

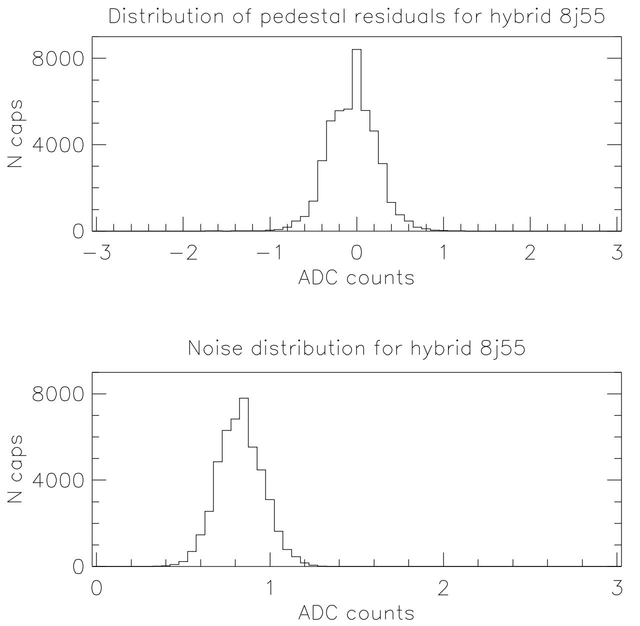
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in