Hybrid 8j56 Traveler

January 12, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J56 has die: 051-031 051-032 051-036 051-037 068-028 068-029 068-030 068-031

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j56 classification info. Created 11:47:09 11/03/99

Hybrid 8j56 quality: fair
Chip classification: unknown -- see plots
Bad channels: unknown -- see plots
Bad cells: none
Random bad capacitors (chip-cell-channel): 3-0-77 3-12-76 3-12-77
   3-13-77 3-17-76 3-17-77 3-18-77 3-20-76 3-20-77 3-22-76 3-22-77
   3-24-76 3-24-77 3-33-76 3-33-77 3-34-77 4-18-84 4-21-29
Channels at pedestal needed for DCMS: 33.6 33.6 33.7 32.7 34.6 33.6 33.6 34.5
```

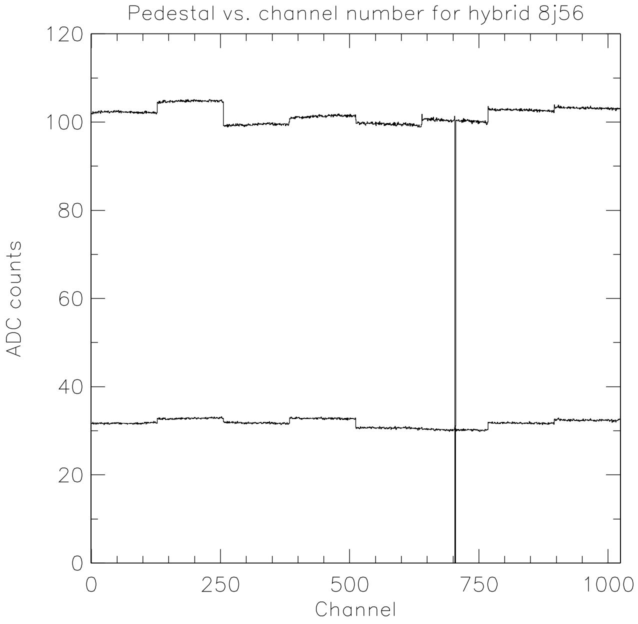
4 Comments

Encountered overcurrents – chip quality information not available – see plots.

5 Pedestal

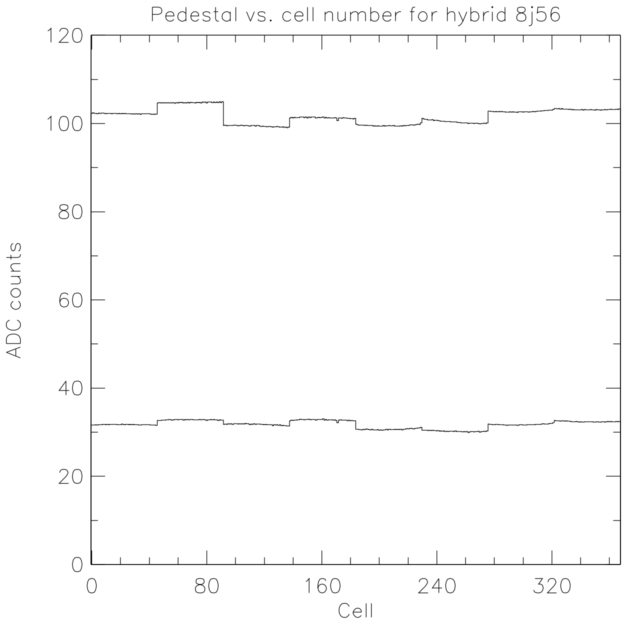
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

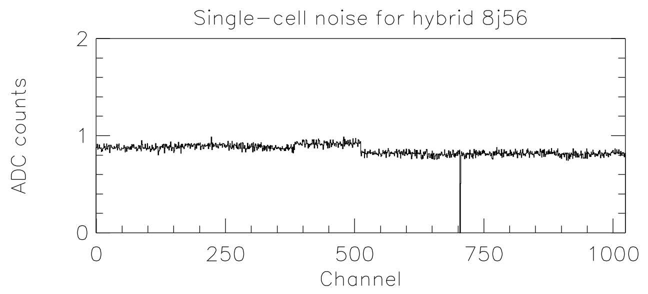
Pedestal vs. Pipeline Cell ID

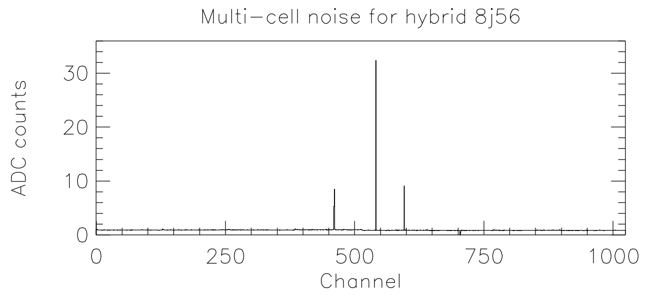


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

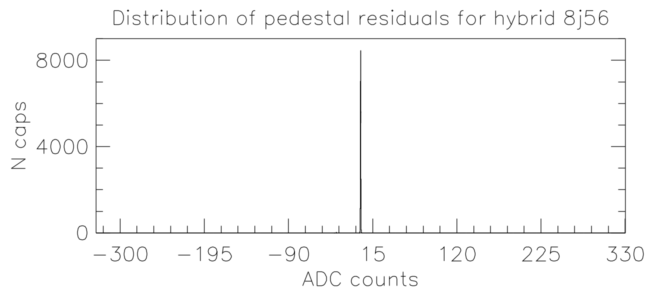
RMS Noise

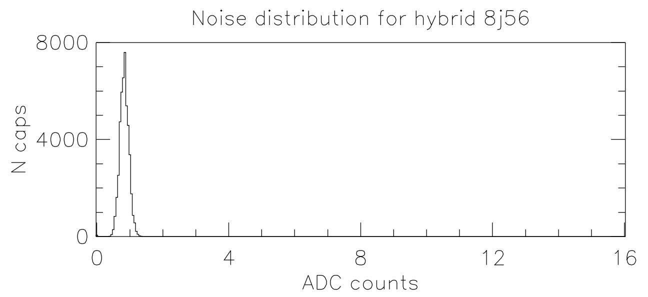




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in