Hybrid 8j61 Traveler

November 9, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J61 has die: 068-004 068-005 068-006 068-007 068-052 066-001 066-002 066-003

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j61 classification info. Created 11:39:10 11/09/99

Hybrid 8j61 quality: fair
Chip classification: fair fair good good fair good fair fair
Bad channels (chip-channel): 0-12 4-37 7-16
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-20-12 1-14-57 1-38-119
   6-15-84 6-15-85 6-16-85 6-2-85 6-28-85 6-4-85 6-42-85 6-45-85
   6-6-85
Channels at pedestal needed for DCMS: 32.6 34.6 34.6 33.7 33.3 35.4 35.6 35.6
```

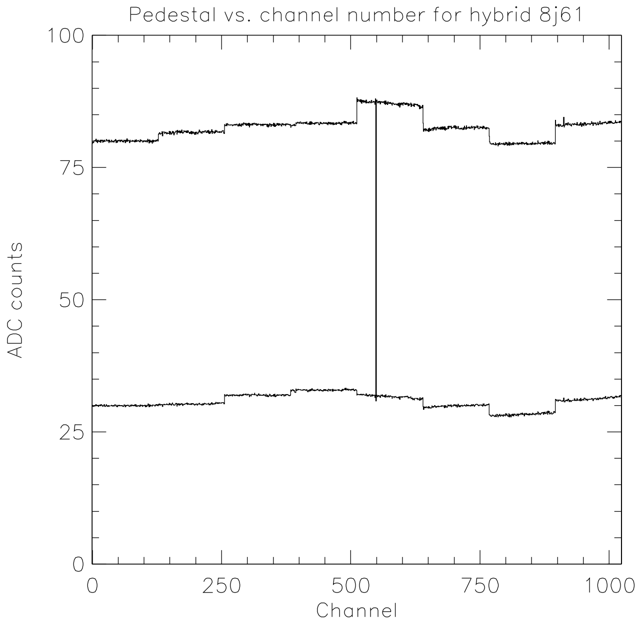
4 Comments

No comments.

5 Pedestal

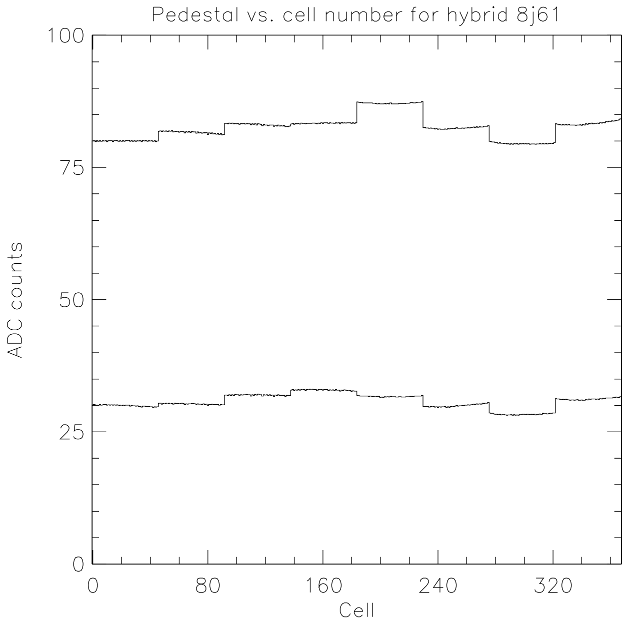
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

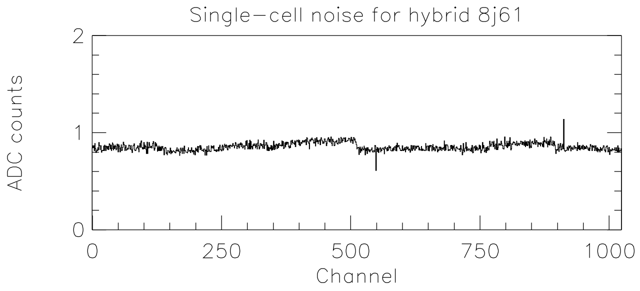
Pedestal vs. Pipeline Cell ID

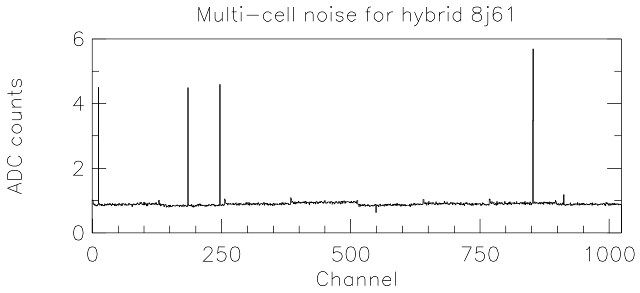


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

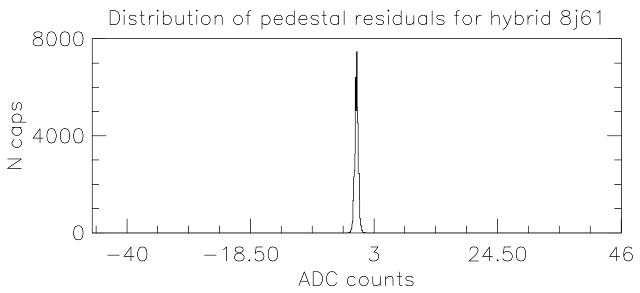
RMS Noise

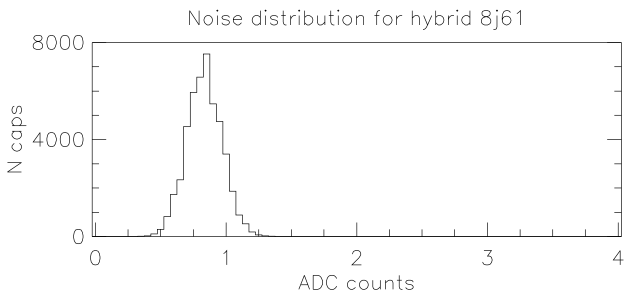




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in