Hybrid 8j65 Traveler

November 30, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J65 has die: 073-036 073-042 073-043 073-044 066-020 066-021 066-047 066-025

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j65 classification info. Created 10:41:15 11/29/99

Hybrid 8j65 quality: fair
Chip classification: good good fair good good good good good
Bad channels (chip-channel): 2-23
Bad cells: none
Random bad capacitors (chip-cell-channel): 2-21-22 2-21-23 2-34-22
   2-34-23 2-35-23 2-38-22 2-38-23 2-39-23 2-41-22 2-41-23 2-43-22
   2-43-23 2-45-22 2-45-23 2-8-22 2-8-23 2-9-23
Channels at pedestal needed for DCMS: 33.7 34.6 34.7 34.6 35.6 35.6 34.6 35.7
```

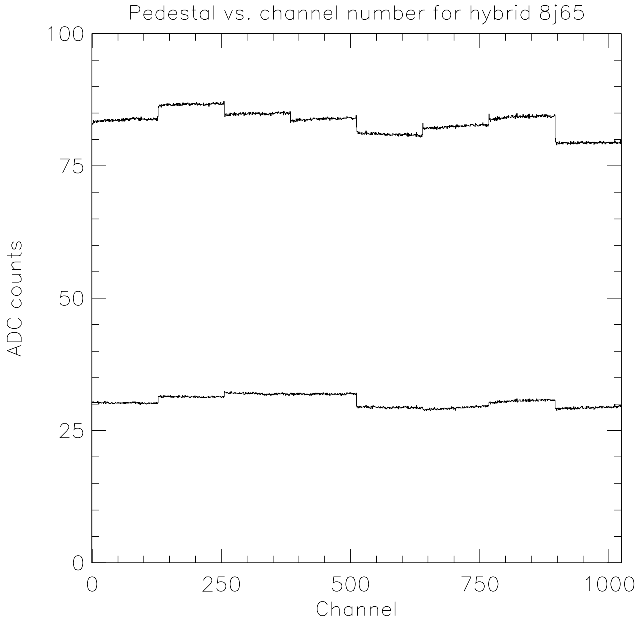
4 Comments

No comments.

5 Pedestal

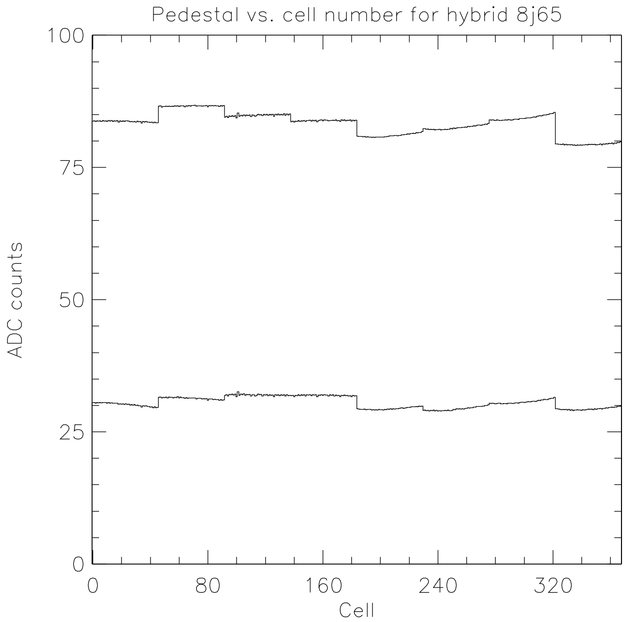
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

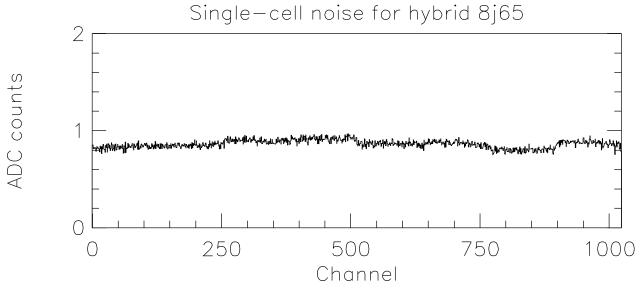
Pedestal vs. Pipeline Cell ID

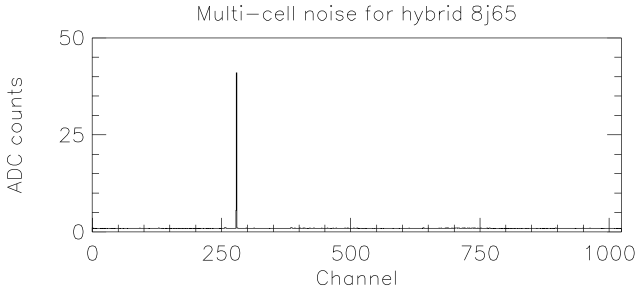


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

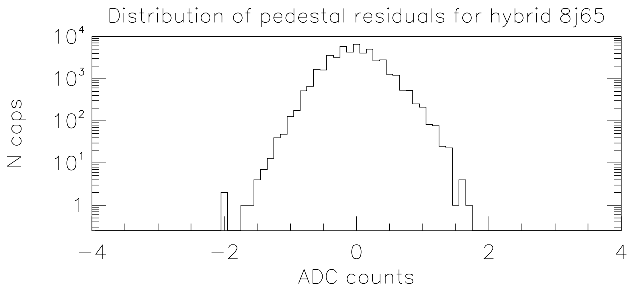
RMS Noise

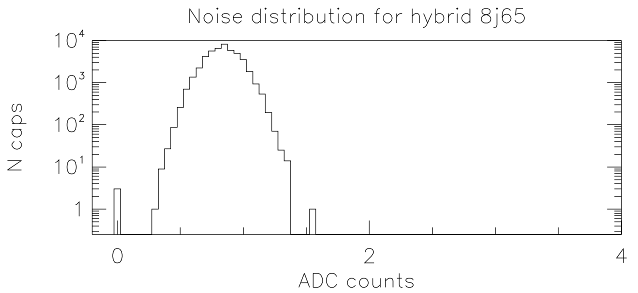




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in