Hybrid 8j73 Traveler

November 23, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J73 has die: 067-025 067-026 067-027 067-028 026-008 026-010 026-011 026-012

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j73 classification info. Created 19:02:13 11/19/99

Hybrid 8j73 quality: fair
Chip classification: fair good good good good fair good good
Bad channels: none
Bad cells: none
Random bad capacitors (chip-cell-channel): 0-0-56 0-1-56 0-10-56
   0-11-56 0-12-56 0-13-56 0-14-56 0-15-56 0-17-56 0-2-56 0-23-56
   0-3-56 0-4-56 0-5-56 0-6-56 0-7-56 0-8-56 0-9-56 5-25-16
Channels at pedestal needed for DCMS: 36.6 35.4 36.1 36.6 33.6 35.1 34.8 33.6
```

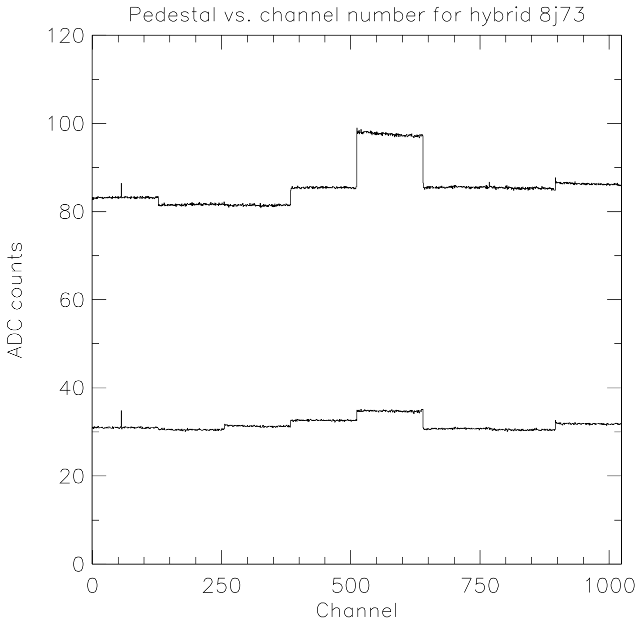
4 Comments

No comments.

5 Pedestal

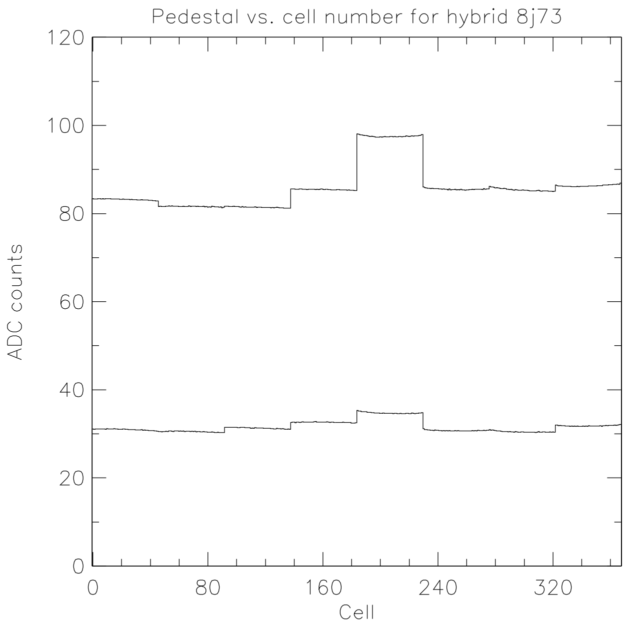
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

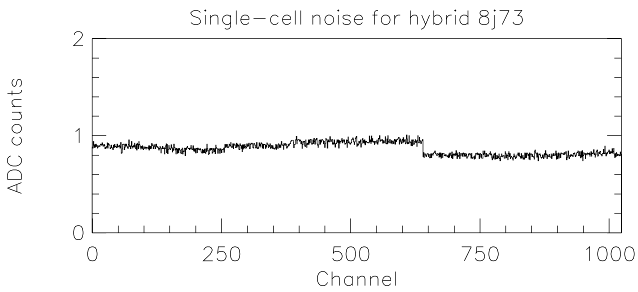
Pedestal vs. Pipeline Cell ID

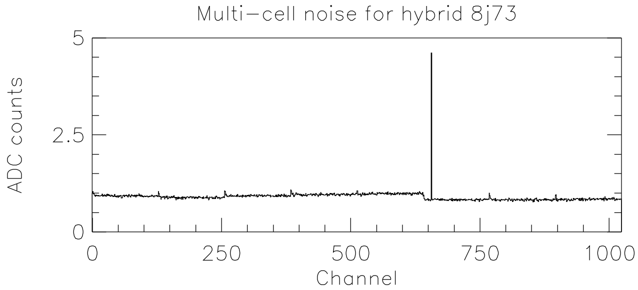


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

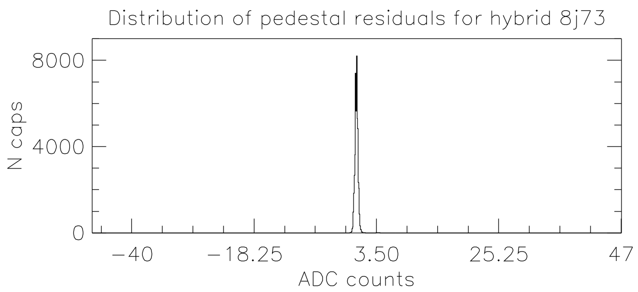
RMS Noise

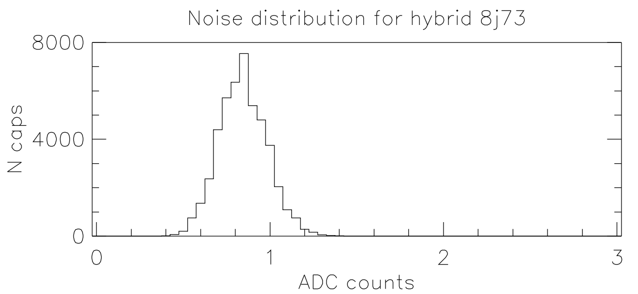




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in