Hybrid 8j75 Traveler

November 30, 1999

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J75 has die: 067-035 067-037 067-038 067-040 026-018 026-019 026-020 026-021

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

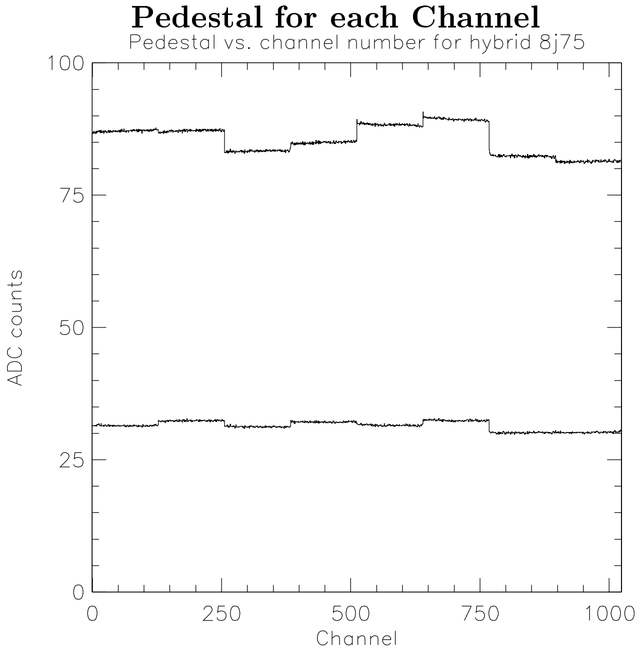
```
% Hybrid 8j75 classification info. Created 10:51:22 11/29/99

Hybrid 8j75 quality: bad
Chip classification: bad bad bad bad bad bad bad bad
Bad channels: N_bad_total = 218 (too many to list all of them)
Bad cells: none
Random bad capacitors: none
Channels at pedestal needed for DCMS: 35.6 35.2 35.6 36.8 32.7 34.2 33.6 35.6
```

4 Comments

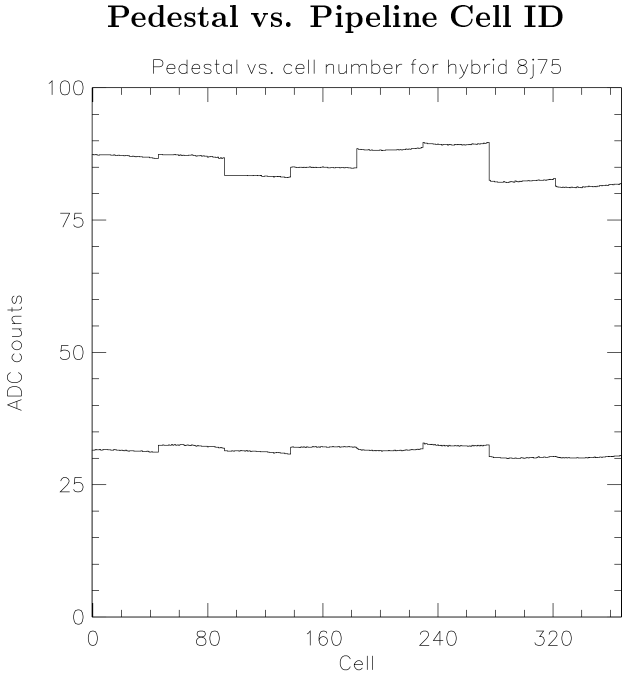
No comments.

5 Pedestal

The following plot shows the pedestals vs. channel number with and without charge injection:



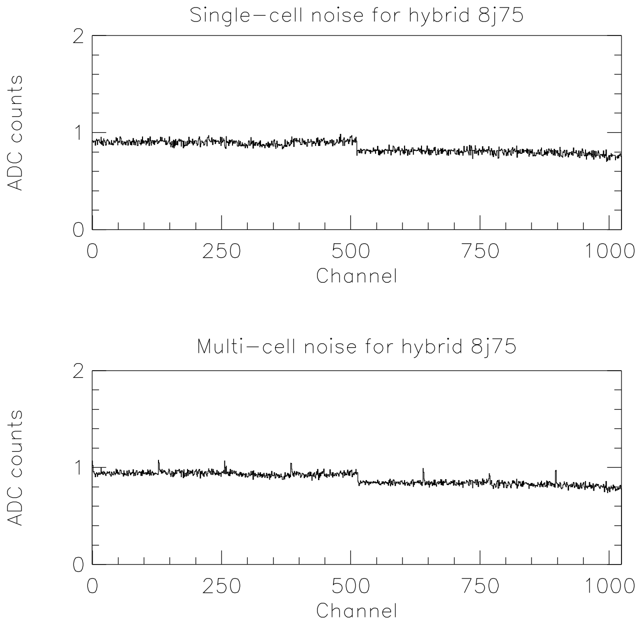
The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.



6 Noise

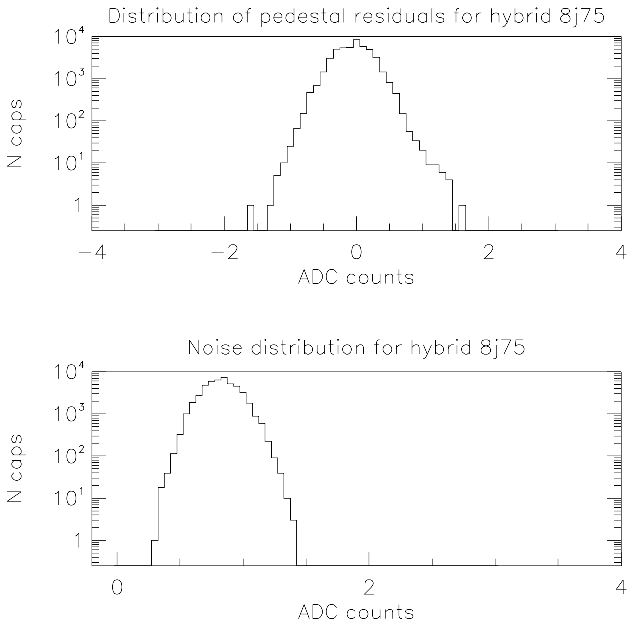
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in