Hybrid 8j80 Traveler

January 4, 2000

1 Connectivity

Repairs on shorts:

Fixes for opens:

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 8J80 has die: 026-048 026-051 026-052 090-002 098-013 098-014 098-016 098-017

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 8j80 classification info. Created 15:56:06 11/22/99

Hybrid 8j80 quality: bad
Chip classification: good good fair good good good bad fair
Bad channels (chip-channel): 2-17 6-1 6-2 6-4 6-9 7-85
Bad cells: none
Random bad capacitors: none
Channels at pedestal needed for DCMS: 33.6 34.7 35.4 35.7 33.6 32.7 34.7 34.4
```

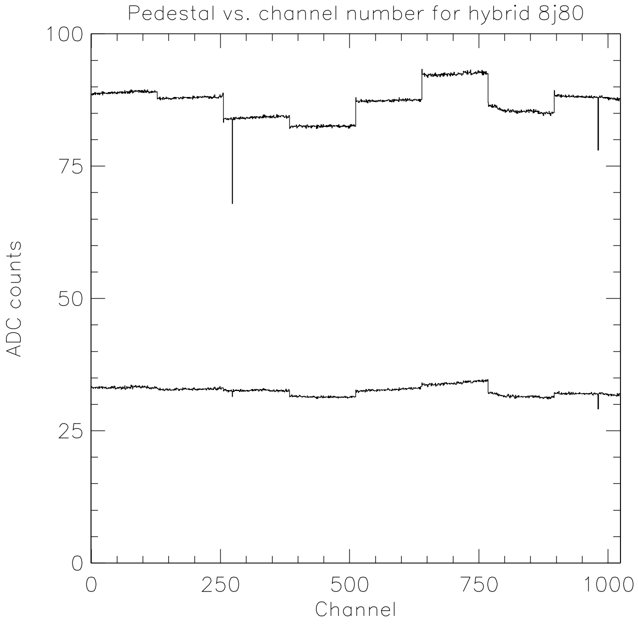
4 Comments

No comments.

5 Pedestal

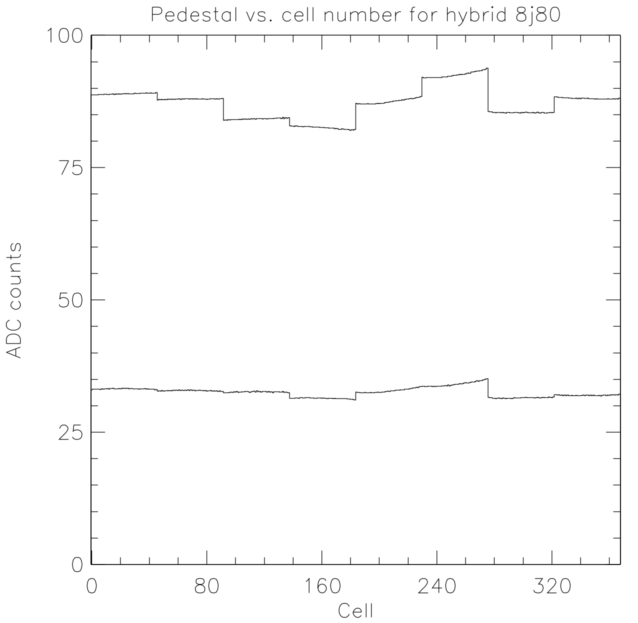
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

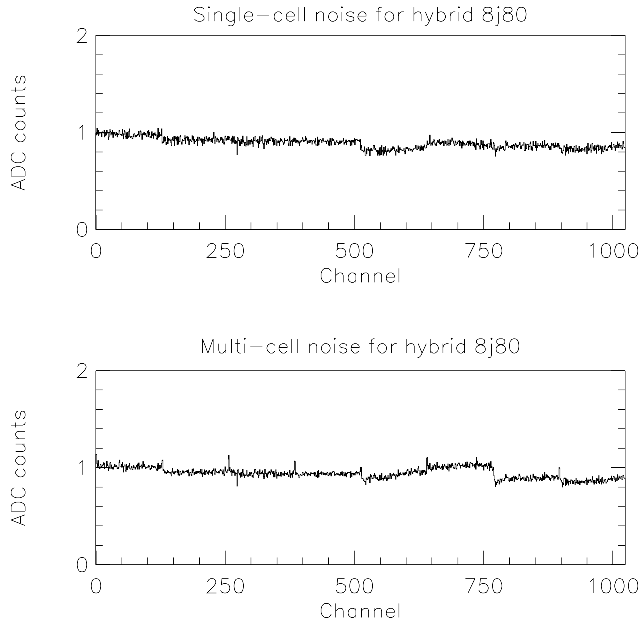
Pedestal vs. Pipeline Cell ID



6 Noise

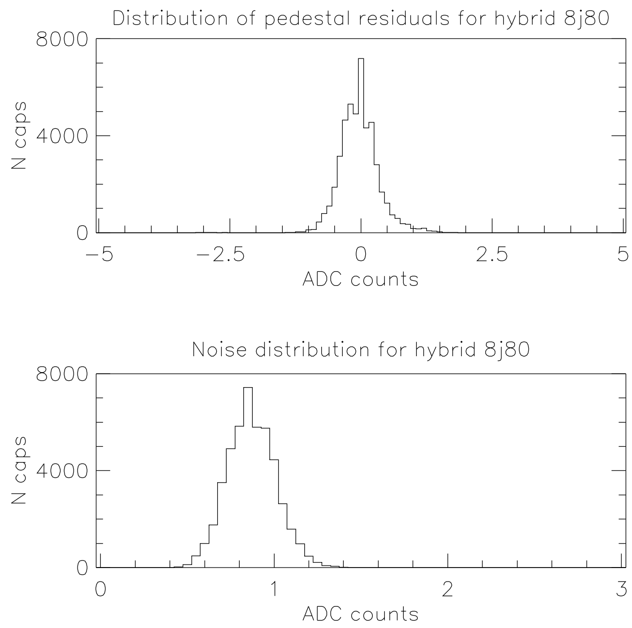
The following plots show the single-cell and multi-cell RMS noise:

RMS Noise



The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise



7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in