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TESTING FRONT-END ELECTRONICS FOR THE CDF SILICON TRACKER UPGRADE

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The upgraded silicon tracker for the Collider Detector at Fermilab has 722,432 strips. These strips are instrumented with SVX3D ASICs fabricated in the Honeywell 0.8 μm radiation hard CMOS process. We describe test setup and procedures used to screen production chips and to ensure reliability of the silicon system front-end electronics.

1. CDF Silicon System Front-End Electronics

For Tevatron Run II, the Collider Detector at Fermilab (CDF) will use an upgraded silicon tracker with increased geometrical acceptance and channel count. Charged particles will traverse one layer of single-sided and up to seven layers of double-sided silicon strip sensors which will provide both r-ϕ and r-z measurements of track coordinates.[1] The sensor strips will be read out with the radiation-hard CMOS application specific integrated circuit (ASIC) called SVX3D. Main features of this ASIC are listed below:

- 128 input channels, 8-bit Wilkinson ADC and digital readout
- Designed to operate with 132 ns or 396 ns bunch crossing rate
- Equivalent noise charge is 700 + 53 electrons/pF in the 132 ns mode
- Deadtimeless operation, 46 cell analog pipeline
- Analog buffers store up to 4 events for subsequent digitization
- On-chip sparsification and common mode noise suppression

A detailed description of the SVX3D circuit design and architecture may be found elsewhere.[2,3,4] The chips are mounted on ceramic hybrids which provide all necessary interconnections and cooling. The hybrids are connected to the so called port cards[5] with a high density copper-on-kapton printed cable; port cards provide power and control signals to the chips and transmit the data outside the detector volume over optical fiber links.

2. SVX3D Test Setup

During the development and production cycle of the SVX3D ASIC, it was necessary to establish procedures for design verification, reliability studies, and production testing of these circuits. The conditions under which these tasks had to be accomplished were substantially different from those found in a typical industrial environment. Due to a moderate part count, acquisition of industrial strength automatic test equipment could not be justified. A sample of chips had to be irradiated to characterize deterioration of circuit performance vs. the accumulated dose, and therefore the test setup had to be portable so that it could be used near a high-intensity radiation source or a particle beam. The complexity of the circuit design and a proprietary manufacturing process rendered a priori derivation of SVX3D fault models impossible. On the bright side, the time available for testing was sufficiently long so that detailed check of the design specifications could be performed for all production chips and hybrids. Taking these considerations into account, we found the following setup to be adequate for all testing purposes:

- Custom-built pattern generator/memory board. This board contains pattern and readout FIFOs with clock, parallel I/O computer interface, and some glue logic. It is capable of running continuously or from external trigger.
- Digital I/O level shifters and adapters needed to interface devices under test to the pattern generator board.
- Programmable power supply with GPIB interface.
- Linux PC with several add-on cards for data acquisition and control.[6]

When necessary, this basic configuration was augmented by other equipment. For example, a GPIB controlled probe station was used for wafer probing, and a temperature stabilized enclosure was utilized for accelerated aging studies.

During the development of the test software, special attention was given to the convenience and clarity of data visualization and presentation of results. Quick identification of potential problems "by eye" proved to be extremely useful at early stages of the chip development and testing. An intuitive graphical user interface allowed for effective interaction between the test program and the operator and for rapid development of test sequences. Open Source software packages have been used with great success throughout the whole project:

- Berkeley DB database system[7] was used to store test data and analysis results
- Data visualization employed Histo-Scope[8], BLT[9], and Xfig[10]
- Data analysis: Histo-Scope, CERNLIB[11]
- Report generation: LaTeX[12]
- GUI tools: Tcl/Tk[13] and various Tcl extensions
- Data acquisition code and package interfaces were written in C and Tcl

3. SVX3D Production Testing Procedures

Upon passing wafer-level tests, the SVX3D die were mounted on multichip hybrids. The number of chips on a single hybrid assembly varied from two to eight, with about five chips on average. Therefore, the rate of defective die not found by the wafer probing had to be reduced to a few percent level to ensure an acceptably low rate of hybrid failures. This requirement led to the development of an extensive suite of wafer-level tests which included monitoring of the circuit currents, exercising the pipeline and readout logic for various combinations of initialization bits and timing sequences, measurements of chip pedestals, noise, and gain using the calibration charge injection, *etc.* The tests were scheduled to run in a sequence from the fastest to the slowest, with the ability to interrupt the probing and move on to the next die if a failure happens during one of the early steps. For the tests which involved the analog circuitry (such as gain measurements) the readout could not be unambiguously compared to a set of fixed expected values; the data from such tests were saved on disk and analyzed offline. The test sequence was designed to exercise each IC feature at least once. Although it was not possible to try all combinations of initialization settings and signal timing, the most likely chip operation scenarios were explored in considerable detail. The running time of the full wafer probing sequence was 50 seconds per die and just under two hours for a six inch wafer.

The average on-wafer SVX3D die yield was found to be 53%. Among die tested good on wafer, a few production lots of SVX3D wafers exhibited anomalously high failure rate (up to 10%) due to dicing and, perhaps, handling. The reason for these failures was not completely understood, but a chip reprobing procedure was instituted to handle die from such lots.

The testing continued after the hybrid assembly. First, the hybrid functionality was checked using a procedure similar to that used for the die in wafers. Due to various assembly and part defects the success rate for this test was about 80%. The hybrids which passed this test were operated continuously for 48 hours, tested again, and then used in the subsequent production of silicon ladders.

Overall, about 20,000 die and 1,700 hybrids were tested to ensure reliability of the CDF silicon system. ASIC projects of such scale are not uncommon for modern high energy and nuclear physics experiments, and we are likely to see the need for similar IC test setups in the near future.

1. The CDF II Collaboration, *The CDF II Detector Technical Design Report,* FERMILAB-Pub-96/390-E (1996).
2. M. Garcia-Sciveres *et al.*, *Nucl. Instr. and Meth.* A 435 (1999), pp. 58–64.
3. T. Zimmerman *et al.*, *Nucl. Instr. and Meth.* A 409 (1998), pp. 369–374.
4. M. Garcia-Sciveres, *Nucl. Instr. and Meth.* A 392 (1997), pp. 375–379.
5. J. Andersen *et al.*, *The Port Card for the Silicon Vertex Detector Upgrade of the Collider Detector at Fermilab,* FERMILAB-Conf-00/262-E (2000).
6. We used Keithley KPCI-PIO96 digital I/O card, ComputerBoards CIO-DAC02/16 analog output card, and National Instruments PCI-GPIB controller. More information about data acquisition with Linux is available from the *Linux Lab Project* home page, http://www.llp.fu-berlin.de/
7. Sleepycat Software, *Berkeley DB embedded database system,* http://www.sleepycat.com
8. Joy Kyriakopulos and Donna Reid, *Histo-Scope V4.0 User's Guide,* http://www-pat.fnal.gov/histo_doc/histo_ug.html
9. George Howlett, *Bell Labs Toolkit,* http://www.tcltk.com/blt/
10. Brian V. Smith, *XFig User Manual,* http://epb1.lbl.gov/BVSmith/xfig/
11. CERN, *CERN Program Library,* http://wwwinfo.cern.ch/asd/cernlib/
12. Leslie Lamport, LaTeX *A Document Preparation System* (Addison-Wesley, 1994).
13. Brent Welch, *Practical Programming in Tcl and Tk* (Prentice Hall, 2000).