# SVX-II Hybrid Electronics

## 1 Introduction

The SVX-II detector is an array of similar modules called “ladders”. A ladder has 4 rectanguar silicon sensors mounted in-line on a common support structure. The 4 sensors are electrically ganged in two independent pairs, with the readout electronics at either end of the ladder. Each ladder end of the SVX-II detector requires two physically separate electronic readout packages, known as hybrids, one on each side of the silicon (Figure 1). The hybrids must be single-sided and separate because they are mounted directly on the silicon sensor surface. After the “phi” and “z” hybrids have been attached to an SVX-II sensor, they are interconnected through an “SVX-II Jumper”, which is a passive device attached to the edge of the sensor (the two sides of a sensor are designated as phi and z). This allows each ladder end be served by a single cable, which is pre-attached to the phi hybrid. SVX-II hybrids contain the following separately fabricated parts, which can be seen in Figure 2:

1. Thick film on beryllia ceramic substrate (“base hybrid”).
2. Multiple SVX3D custom integrated circuits (chips).
3. SVX3-Finger thick film on alumina circuit (one per chip).
4. Surface mount passive components.
5. Soldered copper on kapton flex cable (phi hybrids only).

A close-up of an SVX3-Finger is shown in figure 3. Both the Base Hybrid and the Finger use similar technology but are fabricated independently. This separation accomplishes the following goals:

- The Finger thickness can be matched to the chip thickness, which enables wirebonding in the small space between adjacent chips.
- Due to its small size and lack of thermal function, the Finger can be made on alumina ceramic (the most widely used ceramic in consumer

electronics) which increases the choice of conductor and dielectric materials. The Finger therefore has integral resistors and a capacitor, which are not available for the Base Hybrid.

- The chip spacing is not rigidly fixed by the Base Hybrid artwork, because the fingers are loaded together with the die. This is important for the modular approach, described later.

- The Finger design can be modified to adapt to a new chip design without changing the Base Hybrid. This is advantageous because it is faster and much less costly to produce Fingers than Base Hybrids.

- The fabrication yield of a monolithic hybrid with the same functionality would be roughly the Base Hybrid yield times the $n^{th}$ power of the Finger yield, where $n$ is the number of chips.

## 1.1 Base Hybrids

Since each layer has a different width ladder, a total of 10 hybrid varieties are needed to instrument SVX-II (5 double-sided layers). This presents a design and prototyping challenge, especially since the dead-timeless operation of SVX3D chips located on the active sensors is sensitive to details of the hybrid layout. The SVX-II Base Hybrids follow a modular design in response to this challenge. Every Base Hybrid type is made of a combination of two unit cells: a 2-chip cell and a 3-chip cell. The composition of the 10 Base Hybrids in terms of these unit cells is shown schematically in Figure 4. The cells are combined at the layout stage and thus, once fabricated, a 5-chip Base-Hybrid cannot be cut apart into a 2-chip Base Hybrid and a 3-chip Base Hybrid. What is accomplished by the modular approach is a reduction of the effort to generate the layouts and, more importantly, a vast simplification of the development and prototyping process. This is because conclusions from testing a prototype of a particular hybrid type can be applied to the other nine. However, the hybrid design was constrained to match existing sensor and mechanical designs, and in this context the modular layouts added some complication to both hybrid and ladder assembly. The main reason is that the sensor strip pitch varies from layer to layer, which is not ideal for a modular approach. This forced the use of specialized fixturing to place the

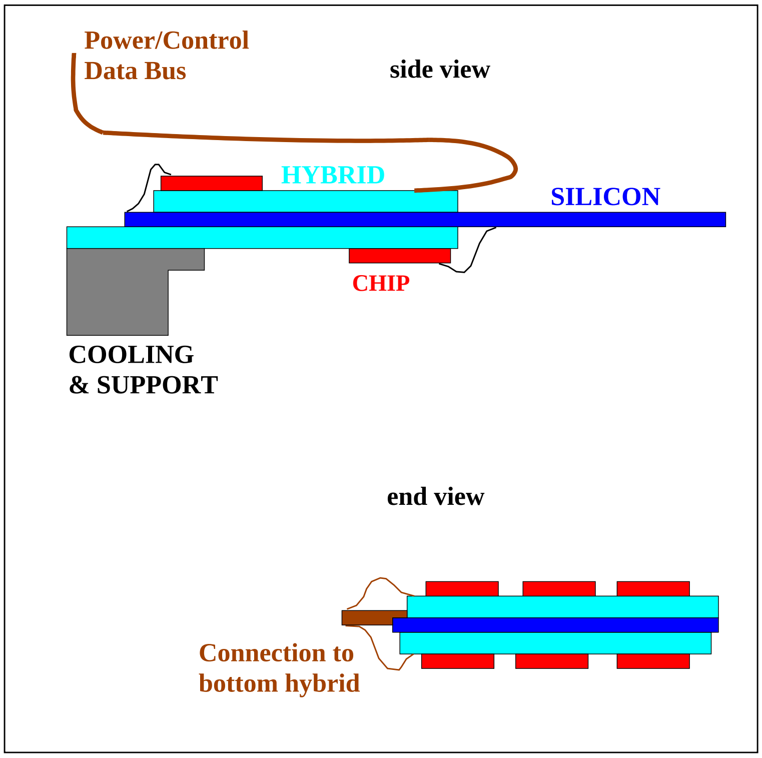


Figure 1: *Diagram of an SVX-II ladder end, showing the silicon "sandwiched" by two hybrids, which are interconnected through an SVX-II Jumper, shown on the end view only. and post-assembly.*

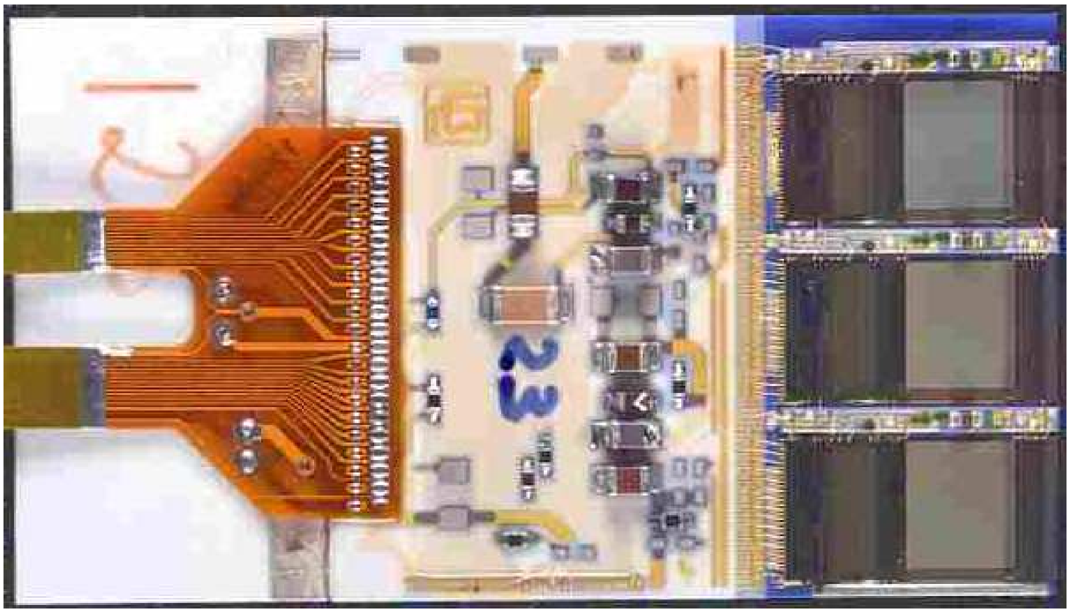

Figure 2: *Photograph of an SVX-II phi hybrid for layer 1. Three SVX3D chips can be seen on the right while the soldered flex cable is on the left.*

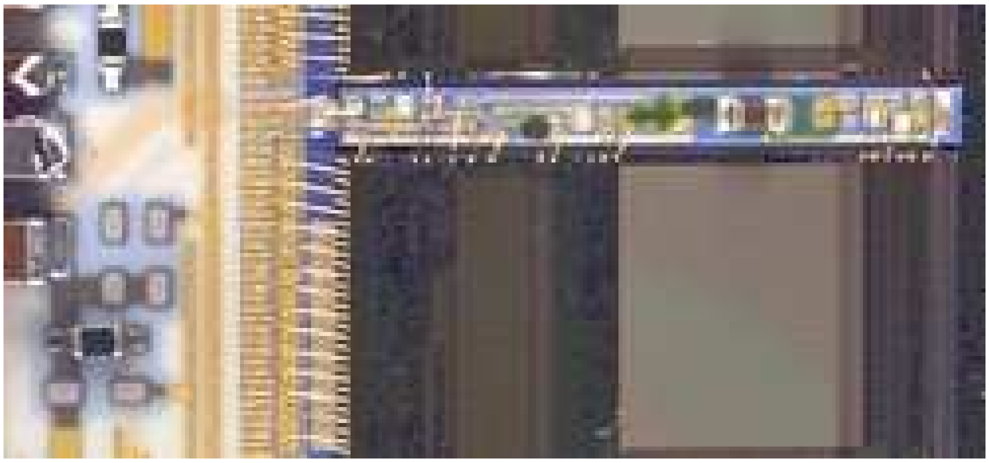

Figure 3: *Close-up photograph of an SVX3 Finger serving the SVX3 chip which appears below it.*

SVX3D chips on the base hybrids with variable spacing depending on layer, and even then systematic offsets in chip placement impacted chip to sensor wirebonding.

## 1.2 SVX3 Fingers

The Fingers are thick film on ceramic circuits like the base hybrids, but they have circuitry on both sides of the ceramic with via interconnections through the ceramic itself. There is one universal finger design for all hybrids, as it is matched to the SVX3D chip, rather than to a specific layer. The finger dimensions are 0.040" $\times$ 0.480", which make it unusually small for thick film technology, Still, thanks to a compact layout it contains, in addition to power bussing, an integral capacitor which takes up most of the back side (16 nF value) and three printed resistors on the front side. The finger can thus be regarded as a custom surface-mount passive component.

All connections between a finger and the corresponding chip are wirebonds, while connections between finger and base hybrid are both wirebonds and silver epoxy. The bottom of the finger has two regions of exposed conductor which are connected to the base hybrid using silver epoxy- which also serves to mechanically hold the finger on the hybrid. One larger region is a ground contact, while a small region at one end (the "heel") is analog power. Fingers must be precisely placed on the base hybrids to keep the silver epoxy under the two regions from touching. Since the two regions are separated by a dilecric gap approximately 2.5mm wide, this was not particularly difficult. A more frequent problem was that the heel contact is small enough that the silver epoxy joint between it and the base hybrid is fragile and can fail. Fingers with bad heel contacts occurred at low (less than 1%) but noticeable rate.

## 1.3 SVX-II Jumpers

The Jumper is not a component of the hybrids themselves

## 1.4 SVX3D Chips

The SVX3D chip is the only active component of the SVX-II hybrids and is a rich subject in its own right. This section is limited to some remarks significant to the hybrid assembly and testing. The design and performance

| Run Start Date | End Date | Hybrid Types | Plates Started | Plates Accepted |
|---|---|---|---|---|
| 7/7/98 | 11/30/98 | L0, L3 | | |
| | | L1, L2 | | |
| | | L4 | | |
| | | L0, L3 | | |
| | | L1, L2 | | |

Table 1: Summary of fabrication runs for base hybrids. The unit of fabrication is one plate, which contains artwork for two $\phi$-hybrids and two Z-hybrids, except for Layer 4, in which case there is only one $\phi$-Z pair per plate. Every run has a single plate design containing all the hybrid types listed.

of the SVX3D chip are described in references [2], [3], and [4]. The test methods and results for wafers and chips are described in references [5] and [6].

# 2 Component Fabrication

## 2.1 Base Hybrid Fabrication

The base hybrids were fabricated by layering thick film conductors and dielectrics on one side of 3.4" square, 0.020" thick Beryllia substrates. The manufacturing took place at Advanced Packaging Technology of America (APTA- San Diego, CA) between July 7, 1998 and May 22, 2000, as detailed in Table 1. The blank substrates were purchased from CBL Ceramics (UK) under the proprietary name Beramic Z, and are 97.9% BeO with ZrO and MgO additives. The composition of the thick film layers is given in Table 2, and further parameters for the conductor layers are given in Table 3. The radiation thickness of the hybrids is calculated in Ref. [1].

The base hybrids use a combination of two different dielectric technologies and two metal systems (silver and gold). Silver and gold metal combinations are typically used in industry to reduce cost by minimizing gold content. Typically the inner layers and vias are made using silver while the top (component) layer adds gold for wirebonding. In the case of the SVX-II base hybrids gold is used in the three upper conductor and via layers, and silver

| Layer | Type | Material | Thickness ($\mu$m) | Part Number |
|---|---|---|---|---|
| BD1 | back cover | dielectric tape | 65 | ESL 41020 |
| FC1 | shield | silver conductor | 8 | ESL 9695 |
| FD1 | insulator | printed dielectric | 40 | ESL 4913-G |
| FC2 | power plane | silver conductor | 10 | ESL 9695 |
| FD2 | insulator | printed dielectric | 40 | ESL 4913-G |
| FC3 | ground plane | silver conductor | 10 | ESL 9695 |
| FD3 | insulator | dielectric tape | 65 | ESL 41010 |
| FC4 | signal traces, bonding pads | gold conductor | 8 | ESL 8835-1B |
| FD4 | insulator | dielectric tape | 65 | ESL 41010 |
| FC5 | signal traces, bonding pads | gold conductor | 8 | ESL 8835-1A |
| FD5 | insulator | dielectric tape | 65 | ESL 41010 |
| FC6 | solder pads and traces | palladium and gold conductors | 10 | ESL 5837 and ESL 8835-1B |
| FO1 | top cover | printed overglaze | 15 | ESL 4904 |

Table 2: Thick film layers on base hybrids. Except for BD1, all layers are on top of the substrate starting with FC1 directly on the ceramic. Via layers, which accomplish inter-layer connections have been omitted for brevity. The wirebonding pads to connect to the SVX3D chip are on layer FC4, while the wirebonding pads to connect to the SVX3 Finger are on FC5. ESL stands for Electro Science Laboratories (PA).

| Layer Type | Layer List | Min. feature ($\mu$m) | Min. pitch ($\mu$m) | Other |
|---|---|---|---|---|
| Silver plane, trace | FC1, FC2, FC3 | 200 | 400 | |
| Printed dielectric via | FD1, FD2 | 200 | 600 | |
| Gold trace 8835-1B | FC4, FC6 | 100 | 200 | gold bond |
| Gold trace 8835-1A | FC5 | 100 | 200 | alum. bond |
| Tape dielectric via | FD3, FD4, FD5 | 100 | 250 | |

Table 3: Parameters of conductor layers on base hybrids. "Gold bond" and "alum. bond" refer to the type of wirebonding that the material is designed for.

is used in the lower power and ground planes in order to minimize radiation length [1]. There are a number of dielectric systems used in industry and they are not typically used in combination. For the SVX-II base hybrids a laminated tape dielectric was used in the fine feature layers because it allowed for higher via density; however, a screen printed dielectric was substituted between power and ground planes in order to minimize the bow of the finished parts. Both these deviations from standard industry practice introduced unexpected problems during manufacture.

The combination of gold and silver inks caused an effect known as "blistering". After each screen printing step the parts are fired at temperatures of the order of $800^{o}$C. At these temperatures arrangements of dissimilar metals and dielectric can give rise to chemical reactions that release gas ("battery effect"). Whenever a part that contains gold and silver inner layers is fired any gas released will be trapped and form bubbles in between dielectric layers, resembling blisters. Blisters, if large enough, can produce shorts and opens as well as delamination of upper metal layers. The blistering effect caused a significant yield loss in the earlier SVX-II base hybrid manufacturing runs. In later runs the effect was reduced (but not completely eliminated) by limiting certain operations to particular furnaces with special temperature profiles, and by subtle changes to the artwork in regions were blistering was consistently observed in many parts. A crucial element for these improvements was the meticulous recording of the processing history of every part (identifiers were placed on the parts at the bare substrate stage). This was not standard practice for the vendor and was implemented and partly carried out by CDF personnel with a regular presence at the vendor. Note that if there is no significant blistering after processing of a given part is complete, there is no risk for blistering appearing later, because during normal use the part will never be exposed to elevated temperatures.

As stated printed dielectric was used to reduce bow. Figure **??** compares the measured profile of test parts consisting of two blank layers of ESL-101 and ESL-102 tape dielectric on blank substrates, respectively. It is clear that ESL-102 (which is a silver-compatible dielectric) is particularly bad. To solve this problem a silver-compatible printed dielectric was used instead of ESL-102 wherever possible, and a blank layer of ESL-102 was added to the back-side of the hybrids in order to compensate the stress of the layers on the front. Printed dielectrics result in a thinned layer than tape dielectrics, and additionally tests determined that for equal thicknesses the printed material produced less bow. The Profile of a Layer 4 production hybrid plate is also included in Figure ?? for comparison. Given the number of layers in a production hybrid the improvement is quite clear. However, the use of printed and tape dielectric systems combined led to a 60% yield loss of an early manufacturing run. The problem was that different methods are used for the layer-to-layer alignment with each dielectric system, and a method for carrying over the from printed dielectric to tape dielectric was not developed in advance. This problem was not anticipated from the small quantity prototype hybrid runs, because for the small quantities it was more convenient and economical to hand-craft several alignment steps rather than assemble a full complement of production tooling. A solution to this problem was obtained by analyzing defective parts and introducing a new step involving a sacrificial part in every run that was built “backwards” (tape dielectric added before printed dielectric, whereas for real parts the printed dielectric comes first) in order to reference the coarse-feature printed dielectric alignment to the fine-feature tape dielectric.

## 2.2 SVX3 Finger Fabrication

The SVX3 fingers were fabricated by layering thick film conductors and dielectrics on both sides of 2.5” square, 0.010” thick Beryllia substrates. Each plate had 160 finger circuits. The manufacturing took place at Promex of Santa Clara, CA between ??? and ???. The first production run failed due to a design error in the use of the combined silver and gold ink system. The design was corrected and a second production run was successful. A third supplemental run was later ordered in order to guarantee enough fingers to produce more hybrids than originally planned. The 95% Alumina substrates were purchased pre-drilled from Applied Laser Technology of Beaverton, OR. Each finger has two 200$\mu$m diameter holes throuigh the substrate that are filled with silver conductor as the first step in thick film printing in order to form power and ground connections to the bottom of the finger. The composition of the printed layers is given in table 4.

Fingers were delivered by the vendor in the form of plates (with 160 parts each). They were electrically tested at LBNL, at which point bad fingers were marked with an ink dot, and the plates were sent for diamond saw dicing. Good fingers were picked directly from the dicing tape by the hybrid assembly vendor. There are 3 printed resistors on each finger. The values of these resistors were controlled by the geometry of the design and by adjusting the thickness of the printed ink during manufacture. The resistor values were

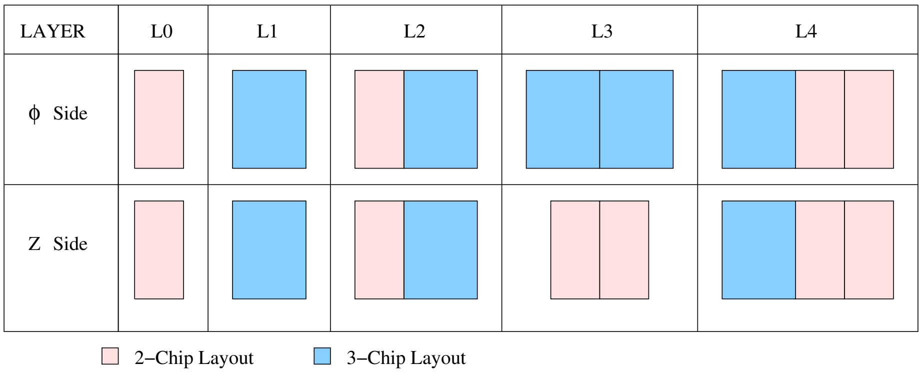


Figure 4: *Diagram showing how the 10 types of SVX-II hybrids are made of combinations of two basic units: a 2-chip layout and a 3-chip layout.*

| Layer | Type | Material | Thickness ($\mu$m) | Part Number |
|---|---|---|---|---|
| BO1 | bottom glaze | printed dielectric | 15 | |
| BM2 | ground bus | silver conductor | 10 | |
| BD1 | capacitor dielectric | printed high K diel. | 40 | |
| BM1 | power bus | silver conductor | 10 | |
| 000 | substrate | alumina ceramic | 250 | N/A |
| TM1 | voltage traces | silver conductor | 10 | |
| TD1 | insulator | printed dielectric | 40 | |
| TM2 | voltage traces | gold conductor | 8 | |
| TR1 | resistors | 10K$\Omega$ / square glaze | 15 | |
| T01 | overglaze | printed dielectric | 15 | |

Table 4: Thick film layers on SVX3 finger. The layers are listed starting with the layers that is physically at the bottom of the part. Note that since this is a double-sided circuit the substrate is listed as a layer in the middle.

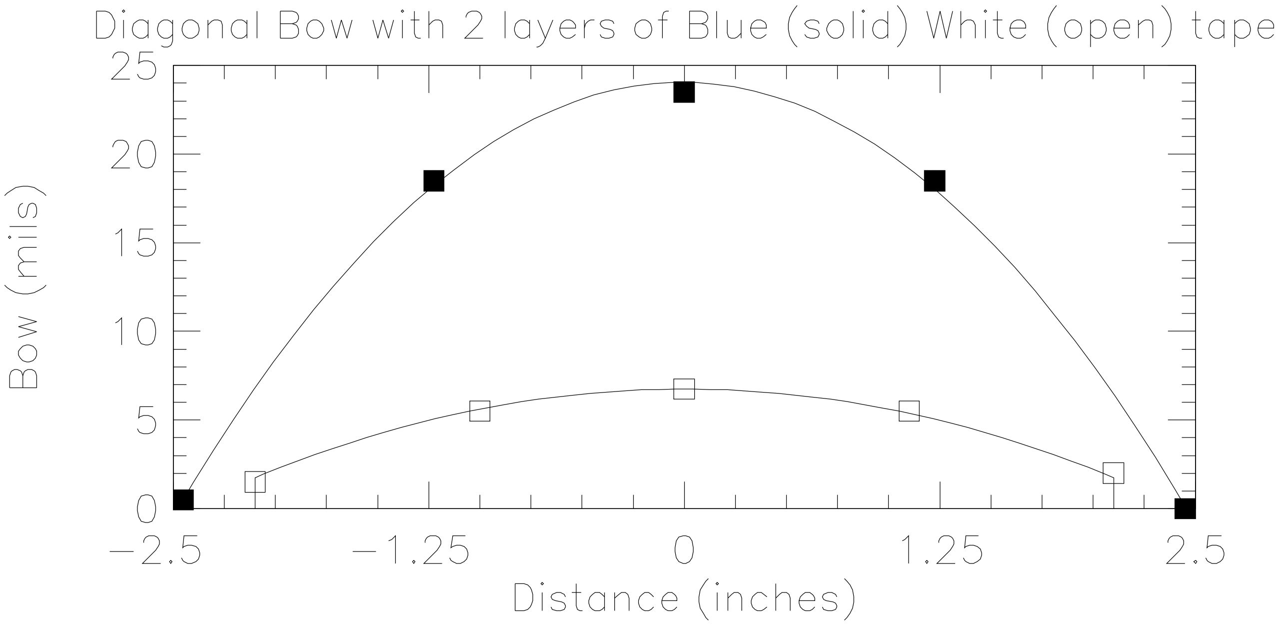


Figure 5: *Measured profile along the diagonal of a 3.5 inch square beryllia plate with lamiated tape.*

measured during testing at LBNL and good/bad parts were classified based on the resulting resistor value distributions (figure 6). For the case of the "dynamic pedestal threshold resistor" the fingers were categorized in two sets: "low resistance", to be used on phi hybrids and "high resistance" to be used on Z hybrids for 90 degree layers. A higher value was desireable for these layers because higher hit occupancy is expected. Some finger plates for which the "as fired" resistor values were generally low were sent to a third party for laser trimming before the electrical tests at LBNL. The resistors are measured in real time during laser trimming, resulting in excellent control of the final value, but note that resistance can only be increased by trimming.

### 2.3 SVX-II Jumper Fabrication

### 2.4 Flex Cable Fabrication

## 3 Assembly and Test

### 3.1 Assembly

The SVX-II hybrid assembly was carried out under contract by Advanced Micro Assemblies (AMA) of Sunnyvale, CA, except for the loading of connectors on the flex cables, which was carried out at LBNL. Additionally the wireonding of about 15% of the parts was done at Zona, Inc. of Sunnyvale, CA and at LBNL in order to compensate from delays at AMA. The assembly steps for SVX-II hybrids are listed in Table 5.

Some of the components used in the assembly sequence of Table 5 required an assembly sequence of their own. Each cable was outfited with two soldered 30-pin connectors and one or two pairs of discrete wires (depending on layer). These operations were carried out by technicians at LBNL. Each finger needed a surface mount capacitor attached to it with silver epoxy prior to loding on the base hybrids. This operation was performed at AMA. The carrier fixtures for the Z hybrids required assembly, including loading a 50 pin connector on a PCB board, or adujustment in order ot recycle a previously used carrier. The number of Z carrier produced was approximately 40% of the number of Z hybrids- about twice the quantitiy originally planned. The Z carrier connector loading was done at AMA, and all other steps at LBNL. The total technician time billed by AMA for all their operations ranged from 1.6 hours for one L0 hyrid to 3.5 hours for one L4 hybrid.

Figure 6: *Distributions of resistor values for the printed resistors on the fingers.*

| Phi Hybrid Step | Z Hybrid Step | Operation |
|---|---|---|
| 1 | 1 | Stencil solder paste on base hybrid |
| 2 | 2 | Manually load surface mount components |
| 3 | 3 | Reflow solder |
| 4 | 4 | Clean with detergent and DI water |
| 5 | | Solder on cable |
| 6 | 5 | Place chips and fingers with silver epoxy |
| 7 | 6 | Cure epoxy |
| | 7 | Load on Z carier fixture |
| 8 | 8 | Gold ball wirebond |

Table 5: Sequence of main assembly steps performed at AMA for SVX-I hybrids. Additional preparatory and post-assembly steps are given in the text.

## 3.2 Component Testing and Yields

An SVX-II ladder end contains a large number of independently fabricated parts. A layer 2 ladder end, for example, contains the following elements, not counting the silicon sensors and mechanical support:

- 10 SVX3D chips
- 10 fingers
- 2 base hybrids
- 1 jumper
- 1 flex cable
- a few dozen surface mount resistors and capacitors

The only way to achieve a high yield for the finished parts, which is mandated by cost and available resources, is to use only componets that are known in advance to be defect-free (Known Good Parts). Achieving a reliable KGP supply for all components in question was a significant challenge (except for surface mount resistors and capacitors).

For commercial applications thick film circuits and other components made by contract vendors are typically used in finished products with a lower level of integration than the SVX-II hybrids, and are produced in large quantities with a low unit cost. This makes it possible to perform exhaustive tests only at the finished product level, at which point defective parts are discarded. Therefore, typical continuity testing and acceptance criteria used by thick film, flex, and other vendors are optimized for speed rather than accuracy. A modest "contamination" of defective components (which will result in some yield loss for finished parts) can be easily tolerated in typical contract assemblies. For SVX-II hybrids it became a apparent at the start of production that this level of testing of the components was not adequate for base hybrids, fingers, or cables. Defective SVX3D chips also made a significant contribution to the initial yield loss of finished hybrids, but in this case the problem was not inadequate testing of SVX3D wafers, but rather latent failure modes present within the chip that resulted in tested good chips turning bad by the time they were loaded on a hybrid. The single chip reprobing necessary to overcome this difficulty is documented separately [6]. For all other components the problem was simply that test methods used by vendors do not result in 100problem was aggravated by the fact that in all cases the component had many features at the limit of the vendor design rules (to take maximum advantage of the technology), which is the point at which manufacturing yield begins to sharply decrease. The higher the fraction of defective parts manufactured, the higher the fraction of bad parts that will pass the vendor acceptance tests.

In order to achieve a supply of known good parts necessary to attain an acceptable yield of finished SVX-II hybrids the following measures were implemented

- All components were re-tested in house after delivery from fabrication vendors.
- Re-tested components were categorized and hand-picked for sending to the assembly vendor to ensure that the best components were used either first or in strategic places (eg. no “fair” chips were used on Layer 0).
- Intermediate test procedures were instituted at the assembly vendor (eg. phi hybrids were tested for shorts immediately after cable attach and then again after chip and finger loading but before wirebonding).
- Work was done with each fabrication vendor to maximize fabrication yield through minor design modifications and to improve their test methods.

  In-house testing of hybrids and fingers was implemented using custom epoxy-ring probecards, a pogo pin custom test fiture, home-made ohmic open and short detectors, and silver paint. Silver paint is a silver-filled temporary conductive coating that is applied as a paint (similar to nail polish) and removed with alcohol. It was used to short together sets of traces at one end in order to test for opens from the other end. Fingers were delivered by the manufacturer in the form of plates containint 160 fingers each. The plates were tested on a semi-automatoc probe station in the same manner as IC wafers. Base hybrids were individually cut and were tested on the pogo pin fixture and on a manual probe station using two different probe cards and to contact different sections. Altogether each base hybrid had to loaded on the probe station 2 separate times and once on the pogo pin fixture to complete all continuity tests. The testing was very accurate and reproducible. Total testing time

| Component | Number from Manufacturer | Perfect Fraction | Usable Fraction |
|---|---|---|---|
| L0 phi+Z base hybrid | 280 | 50% | 80% |
| L1 phi+Z base hybrid | 280 | 50% | 80% |
| L3 Z base hybrid | 140 | 50% | 80% |
| L2 phi+Z base hybrid | 280 | 50% | 80% |
| L3 phi base hybrid | 140 | 50% | 80% |
| L4 phi+Z base hybrid | 280 | 50% | 80% |
| Fingers | 4000 | 80% | 90% |
| Layer 0 cable | 200 | 80% | 80% |
| Layer 1 cable | 150 | 80% | 80% |
| Layer 2 cable | 150 | 80% | 80% |
| Layer 3 cable | 150 | 80% | 80% |
| Layer 4 cable | 150 | 80% | 80% |

Table 6: Summary of in-house testing results for base hybrids, fingers and cables. Base hybrids for the same number of FE chips have been combined. Different production runs have also been combined even though there were run dependent yiled losses.

was approximately 10 minutes per base hybrid. Each failure found was documented, an some classes of common failures that could be repaired were identified. Base hybrids that did not need repairs were sent to the assembly vendor first and others were repaired as needed. In some cases defects were not repaired but accomodated by a adding special wirebonds unique to the specific part. The need for such wirebonds was documented at the time the base hybrids were tested and the wirebonds were added in-house after the pats returned from the assembly vendor. Clearly identification of parts with serial numbers was important. The results of in-house testing are summarized in Table 6.

### 3.3 Assembled Hybrid Testing and Yields

## References

[1] L. Chen and A. Connolly, CDF internal note 5355 (2000).

[2] The SVX3D chip.

[3] The SVX3D chip.

[4] The SVX3D chip.

[5] Testing of SVX3D wafers.

[6] Single chip testing.