# Post-Dicing Probing of SVX3D Chips

Igor Volobouev, Maurice Garcia–Sciveres

Lawrence Berkeley National Laboratory

A total of 1,711 ceramic hybrids were assembled with 8,760 SVX3D integrated circuits (chips) between May 1999 and July 2000 for construction of the CDF-II silicon detectors. The total number of hybrids encompasses 13 different designs containing between 2 and 8 chips each. The characteristics of these hybrids were such that identifying defective chips through hybrid testing after assembly was very difficult, and replacing defective chips involved time-consuming operations and significant risk to the integrity of the part. It was therefore desirable to assemble hybrids using only known good die (KGD).

The initial approach to selecting KGD was to perform exhaustive electrical tests of every chip on a wafer before the wafer was diced. This is the dominant approach used in industry for bare die applications. However, in our initial period of assembly the rate of defective chips on newly assembled hybrids was approximately 30%. Through a series of tests it was determined that a large fraction of these failures were not caused by assembly operations. After experimenting with different dicing techniques and vendors it was concluded that the SVX3D device had latent failure modes that were activated by any handling step, and that there was nothing special about dicing in particular. At this point it was decided to introduce electrical testing of individual chips just prior to use in assembly. This did not completely eliminate defective chips on newly assembled hybrids, as handling is an inevitable part of assembly, but in the end a failure rate of newly assembled chips of 4% was achieved, while the total post-dicing failure rate was 11%. In all, 279 chips were removed from hybrids and replaced (not all hybrids with defective chips were repaired). Figure 1 shows the time evolution of the fraction of chips rejected post-dicing (number of chips that failed post-dicing test over number of chips that were good before dicing and tested after dicing) and the fraction of defective chips found after assembly ("Assembled Fraction Lost").

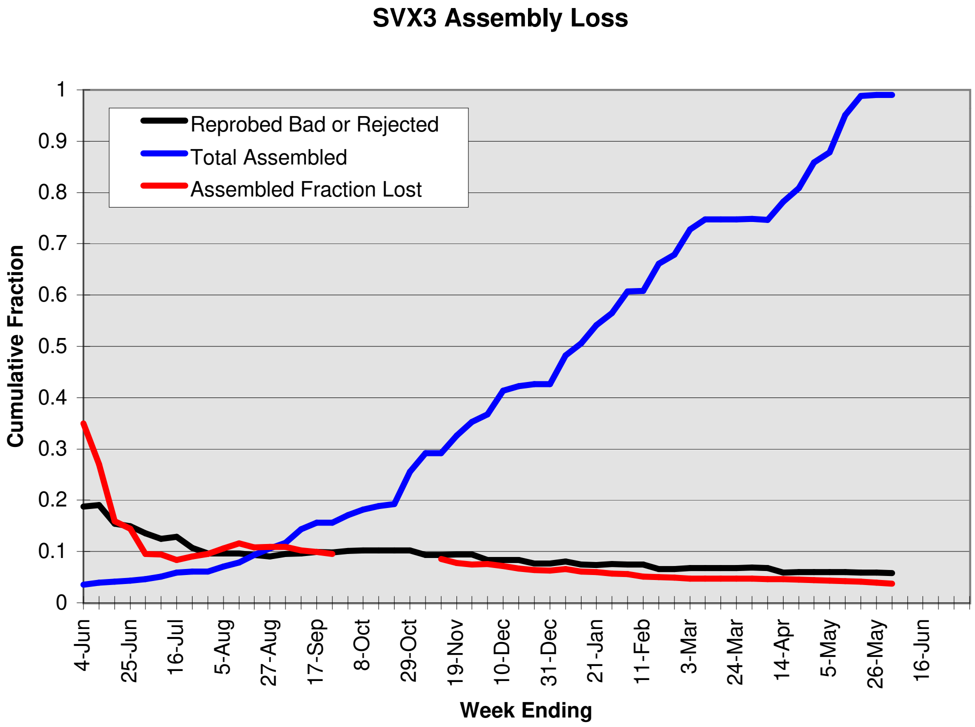


Figure 1: *Time evolution of fraction of SVX3D chips lost post-dicing and post-assembly.*

The post-dicing probing of individual chips was implemented using a holder similar to a die pack, but with built-in vacuum hold-down in each pocket and using precision construction (figure 2). The holder is made of two parts: a laser-cut stainless steel grid attached to a a vacuum base plate that is machined out of aluminum and ground flat. The holder is loaded with 39 chips as they are picked from the dicing tape. Once full, the holder is tilted and gently shaken to allow each chip to fall into the precision location determined by two sides of each cavity. Then the vacuum is applied and the holder is loaded on an automatic probe-station and aligned like a wafer.

However, because the chip edges are not exactly in the same relation to the bonding pads for every chip, the holder cannot yet be probed automatically, as a wafer would. Instead, a control program first steps to the location of each cavity in the holder, showing the image of a bonding pad on the display. Using the arrow keys on the computer keyboard the operator then centers this image and accepts it for each of die on the holder. This fine-alignment process takes less than 10 minutes for a full holder. The control program stores the corrected locations of each chip such that after the fine alignment is complete the holder can be probed exactly like a wafer. The full suite of electrical tests performed on the SVX3D chips took 1 minute per chip. The labor required for post-dicing probing was dominated by the time taken to pick the chips from the dicing tape and load them onto the holder. The total operator time was 1 hour per 39 chips reprobed (the probe station runs unattended during electrical testing).

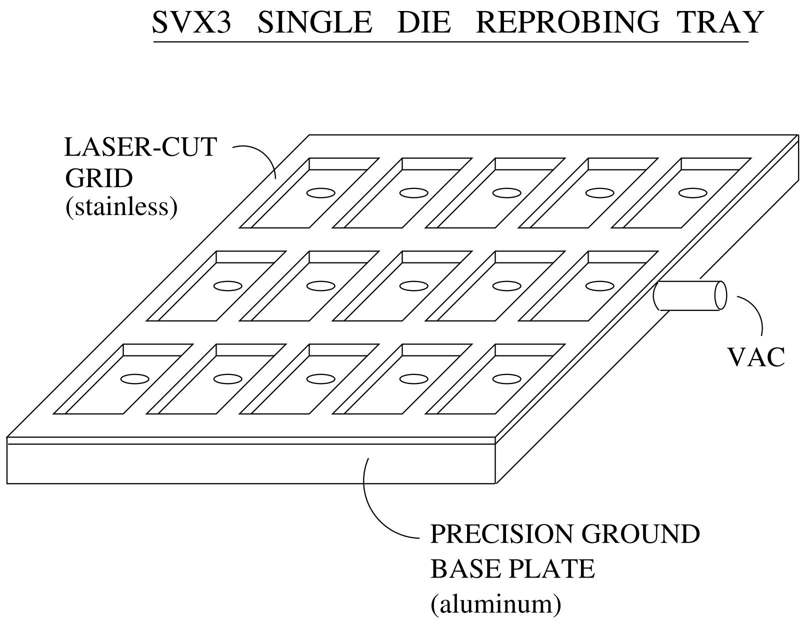


Figure 2: *Schematic of single chip reprobing tray. Actual tray holds 39 chips.*