# Software for the SVT Upgrade

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# Overview

REM:

- will try to work backwards (from upgrade running in crate to now)
- All times in FTEs
- Consulting/Training not included!

- Online
  - DAQ related code
  - Diagnostics
    - "Spy" monitoring
    - Diagnostics
- Offline
  - Configuration (patterns etc.)
  - Simulation (svtsim)
  - Diagnostics on data

# Online

- Entry in board DB
- Coldstart code                    [1 Week/board]
  - Handling of all required registers/memories
  - Configuration files parsers
  - DB hookups, if additional data (I.e. memory fragments) needs to be stored
- Spy monitoring hooks                    [1 week]
  - REM: spy buffers
    - copy input and output data
    - VME accessible data buffers
    - Completely independent from data taking/pipeline activity
  - Read/reset spy buffers

# Online: spy monitoring

- Cope with new boards I/O channels
  - TF: trivial
  - AMS-HB-RW/HB+RW
- Currently put a copy of SB on online disks, would like to have:
  - Easily (ascii file?) choice of buffer dumps      [~week]
  - Higher level automatic/semiautomatic diagnostics:
    - Run board simulation on input and compare with output
                                                    [1-2months]
    - Diagnose trivial issues:
      - BC mismatches, error sources                    [2 weeks]
      - Flaky bits (simulation)
      - Internal de-synch (simulation)

# Board level diagnostics
## what do you use when there's a faulty object?

- **Individual board:**
  - Low level access routines
    [1 week/board]
    - Registers
    - Memories
  - "menu"    [~1 week/board]
    - Read/write registers
    - Onboard memories i/o
  - Test/exerciser program
    [~2 weeks/board]
    - flow data through
    - read/write registers
    - Read/write memories

- **Multiple boards:**
  - Exercise board "blocks"
    - AMS+AM    [2 weeks]
    - AMS+AM+HB
      [2-3 weeks]
  - Exercise test stand wedge    [2-3 weeks]
    - Random hits
    - Fake hits

# Offline

- Pattern Generation
  - Larger number of patterns                    [~days]
  - Alternate sources for XFT layer
    - Muons                                       [1-2 weeks]
    - ?
- Fit Constants
  - "High level"   $\left(\vec{a}\cdot\vec{x}+\vec{b}\right)$
    - Standard SVT→keep same
    - "Muon based"→needs patches to existing code

                                                  [2 weeks]

  - "Low level" (coefficients→memories)           [2 weeks]
    - Need to model on new hardware requirements
    - Cope wit larger number of patterns

# Simulation (in parallel)

- Upgrade to 512K patterns (90% done)      [week]
- Implement board emulator for new individual boards:                              [1 week/board]
  - TF: same (?)
  - RW: new "firmware version"
  - AMS: new "firmware version"
- Implement handling of online configuration files (hwset & mapset) for new/upgraded objects
  
  [1/2 week/board]
- Can evolve in parallel to current svtsim:
  - just build a new instance of svtsimmodule
  - Will be automatically interfaced to the trigger simulation framework!

# Constraints

Now-ish

Conceptual design (specs)

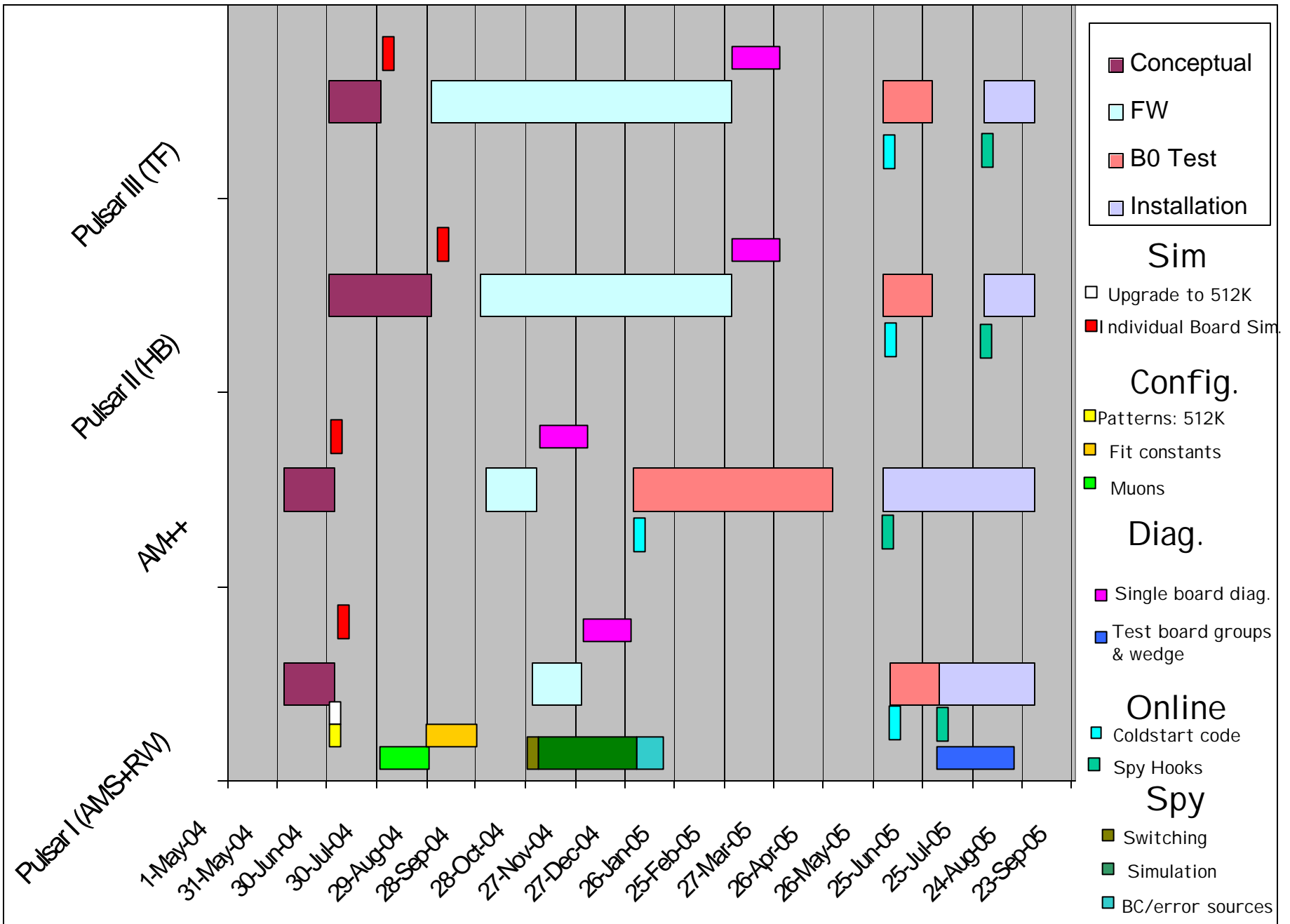Firmware

Hardware

• Diagnostics

• Low level code

• Spy I/o

• Simulation

• Pattern/constants

• High level Spy
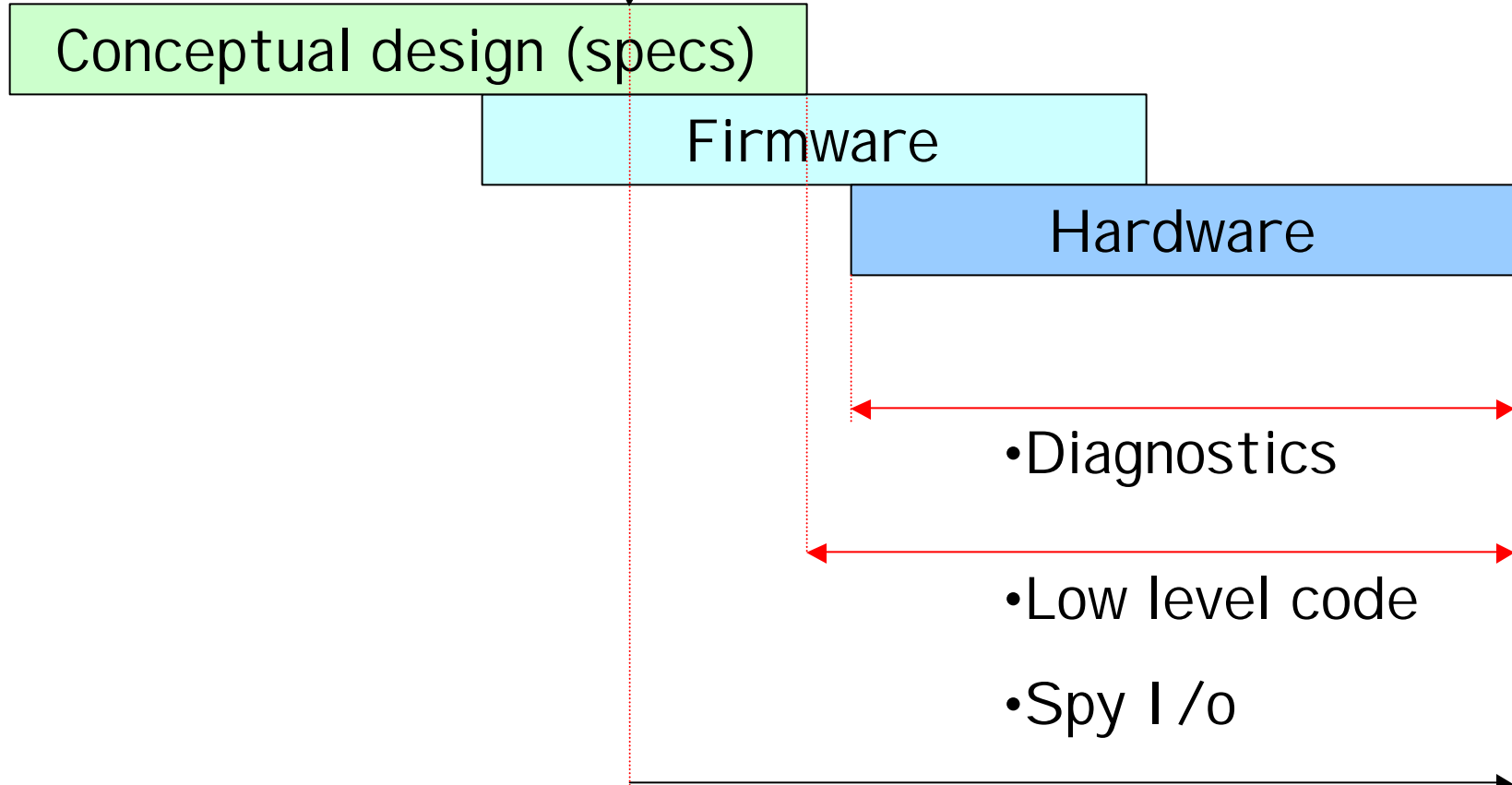
# Resources

## Consultants:

Jahred Adelman,
Stefano Belforte,
Roberto Carosi,
Alessandro Cerri,
Taka Maruyama,
Marco Rescigno,
Un-Ki Yang

## Manpower:

- Board developers
  (ex officio)
- Wisconsin: 4FTE
- A. Cerri
- R. Carosi
- M. Rescigno
- S. Donati

~2FTE?

# A map of "consultants"

| | | |
|---|---|---|
| Offline | Simulation | Alex, Marco, Roberto, Stefano, Taka, Un-Ki |
| | Configuration tools (patterns etc.) | Alex, Pierluigi, Roberto |
| Online | Low level access routines | Alex, Jahred, Marco, Roberto, Stefano, Taka, Un-Ki |
| Diagnostic | Board level | Alex, Franco, Roberto, Stefano, Taka, Un-Ki |
| | Spy | Marco, Subir |
| Infrastructure | DB maintenance (configuration files, HW DB) | Alex, Marco, Roberto, Stefano |