

The SVT Upgrade

- Introduction
- Physics motivation
- Impact of the upgrade

A. Annovi, S. Belforte, P. Catastini, A.
Cerri, M. Dell'Orso, P. Giannetti, L.
Ristori

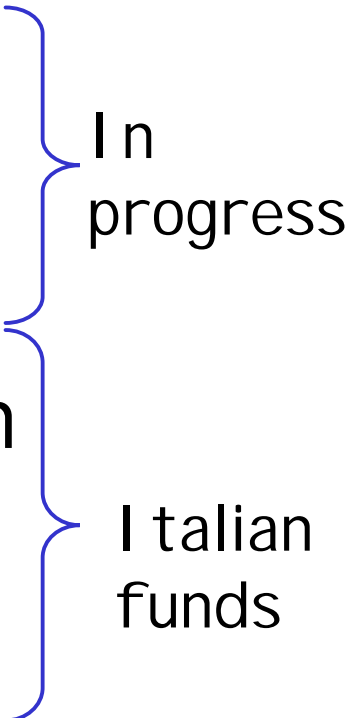
Special Thanks:

M. Schmidt, J. Lewis

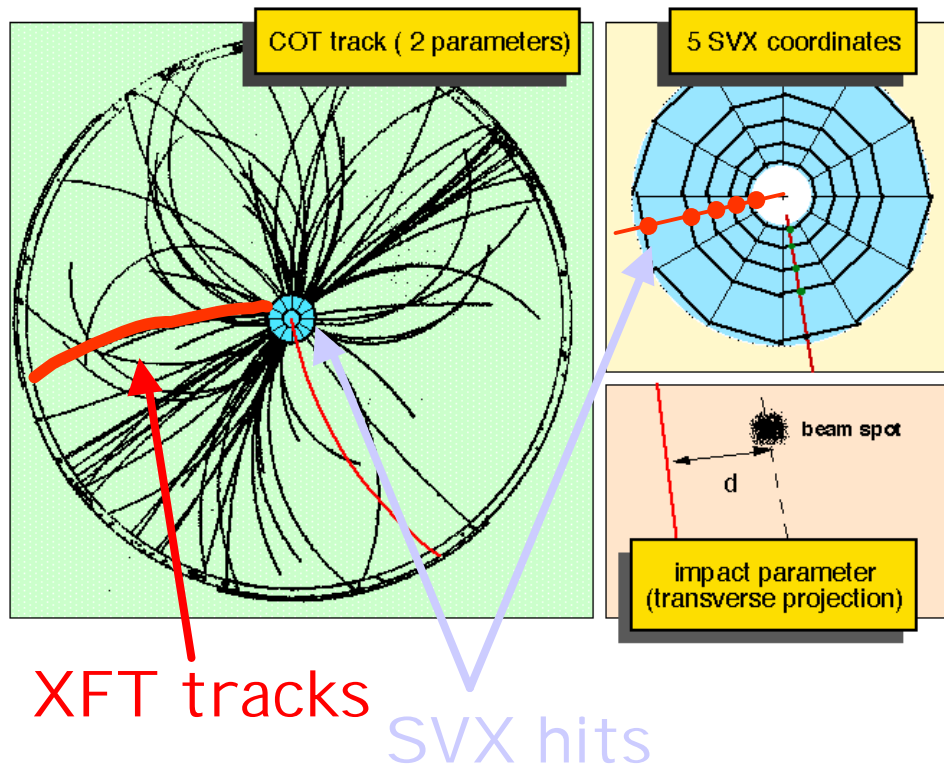
More inclusive list:

Annovi, Bardi, Belforte, Catastini, Cerri,
Dell'Orso, Giannetti, Ristori,
Spinella, Damiani, Sartori,
Tripiccione, Cotta, Chiozzi

What is being proposed

- Addition of a new SVT module: the **Road Warrior** (mostly timing improvements)
 - Replacement of pattern recognition hardware, in particular
32K \rightarrow O(128K) patterns/wedge
- 
- In progress
- Italian funds

SVT: Silicon Vertex Trigger



XFT + SVX 4/4 (until 6/2003)

XFT + SVX 4/5, more efficient

Instead of **XFT**:

m $1 < h < 1.5$

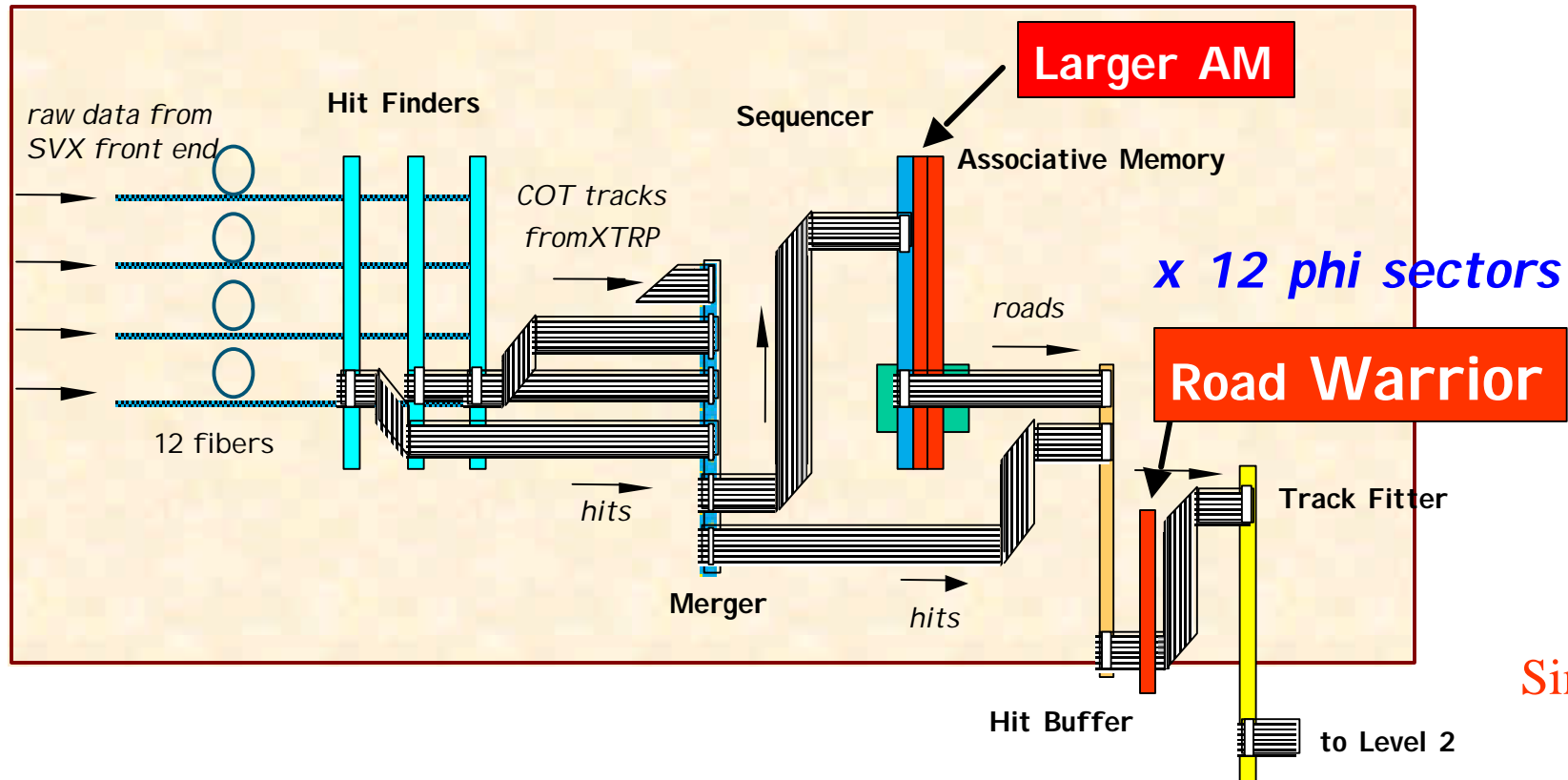
e $1 < h < 2.5$

New Functionalities:

m + SVX 4/5, $1 < h < 1.5$

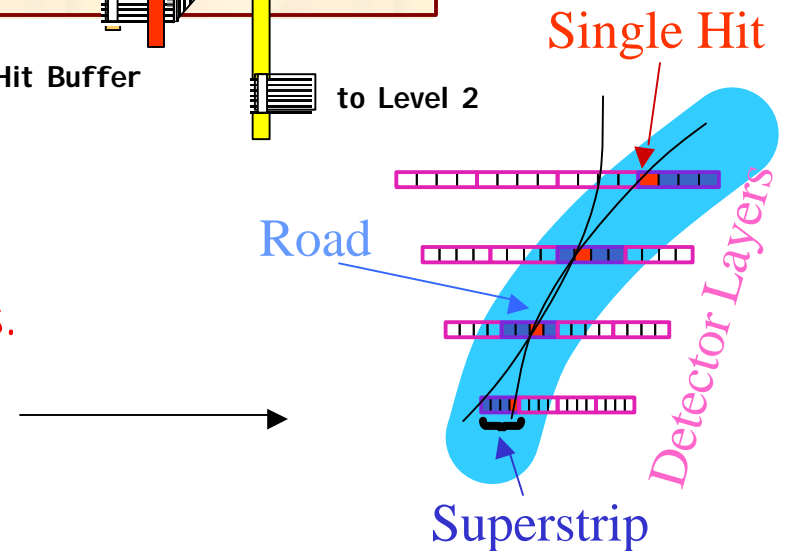
e + SVX 4/5, $1 < h < 2.5$

What does the new Hardware do?



How to speed up SVT:

1. Thinner roads (larger AM) → less fits.
2. Road Warrior → ghosts removal



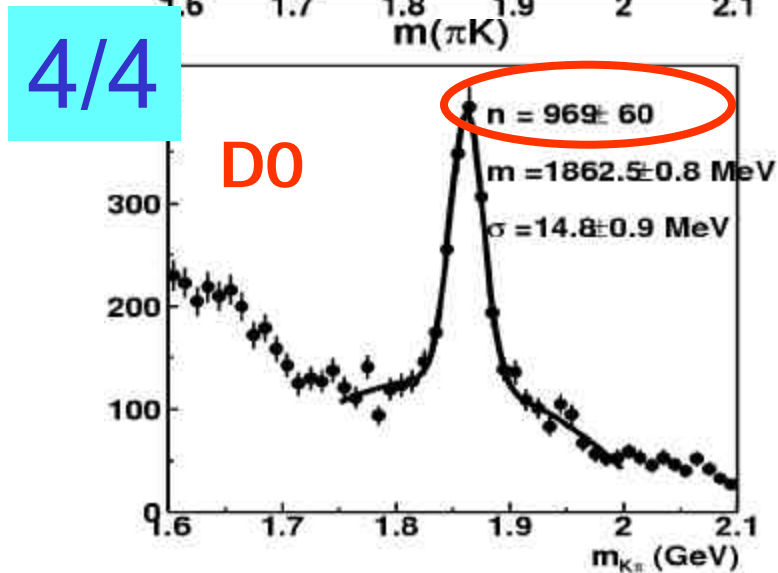
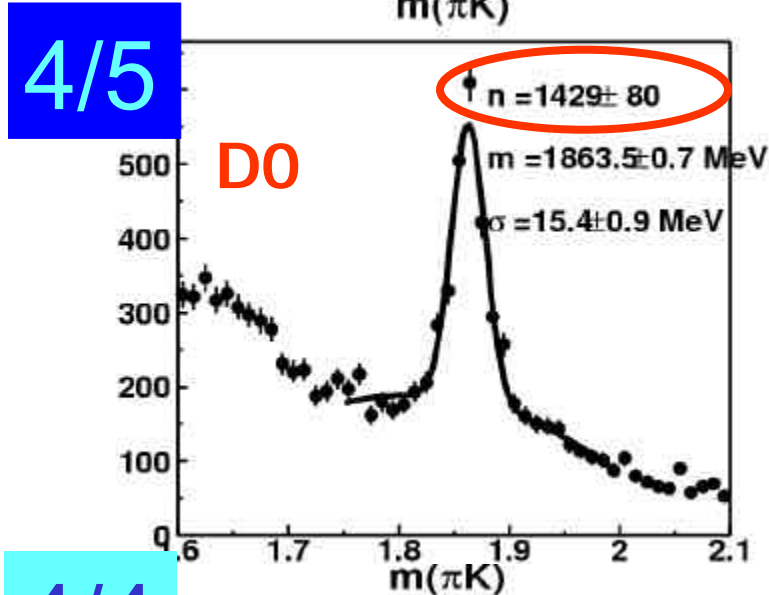
Physics motivations

- We have one fundamental resource:
→ **bandwidth** ←
- SVT is in the critical path for L2 timing/L1 accept rate
- Additional hardware provides better flexibility for trigger design.
Example: **forward muons**

4/4 vs 4/5

Improving the SVT timing

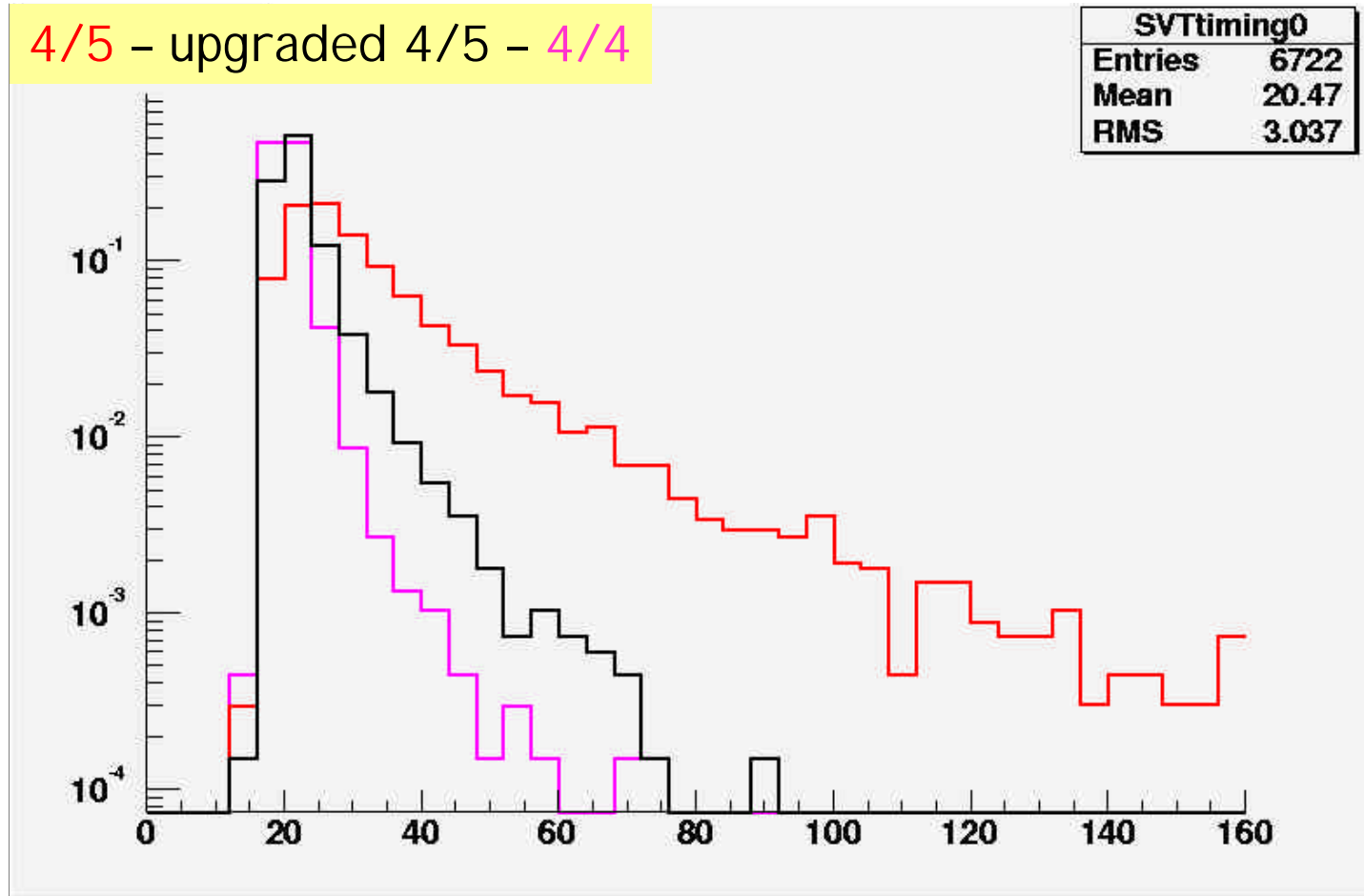
Why do we want 4/5?



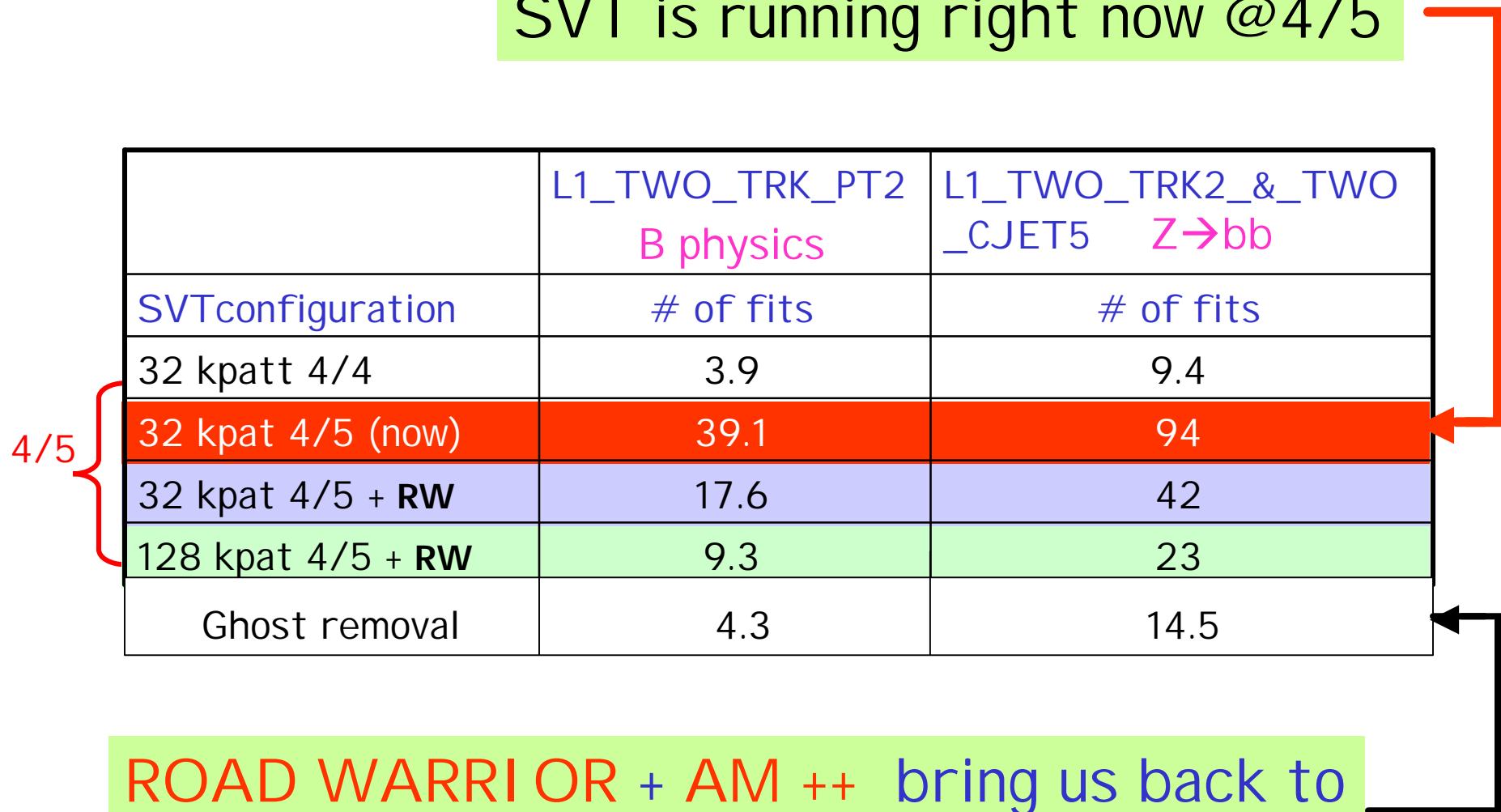
source	4/4	4/5	R
D0 yield	11.2 (nb)	17.5 (nb)	1.55 ±0.06
J/psi yield	663	974	1.5
Bs MC (Pt_b > 5.5; η_b < 1.3)			1.59 ±0.05
Bs MC after offline reconstructi on (Ivan F.)			1.58

Upgrades:
 $T(4/5) \rightarrow T(4/4) !$

4/5 - upgraded 4/5 - 4/4



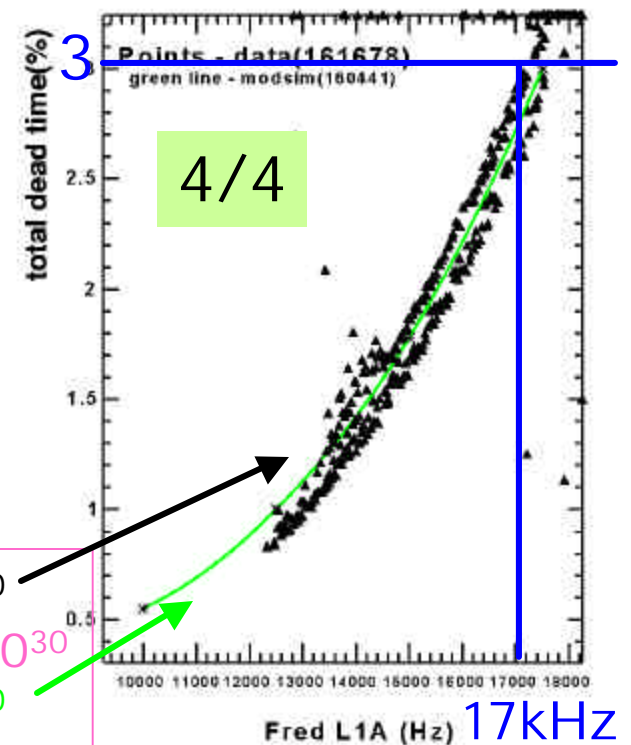
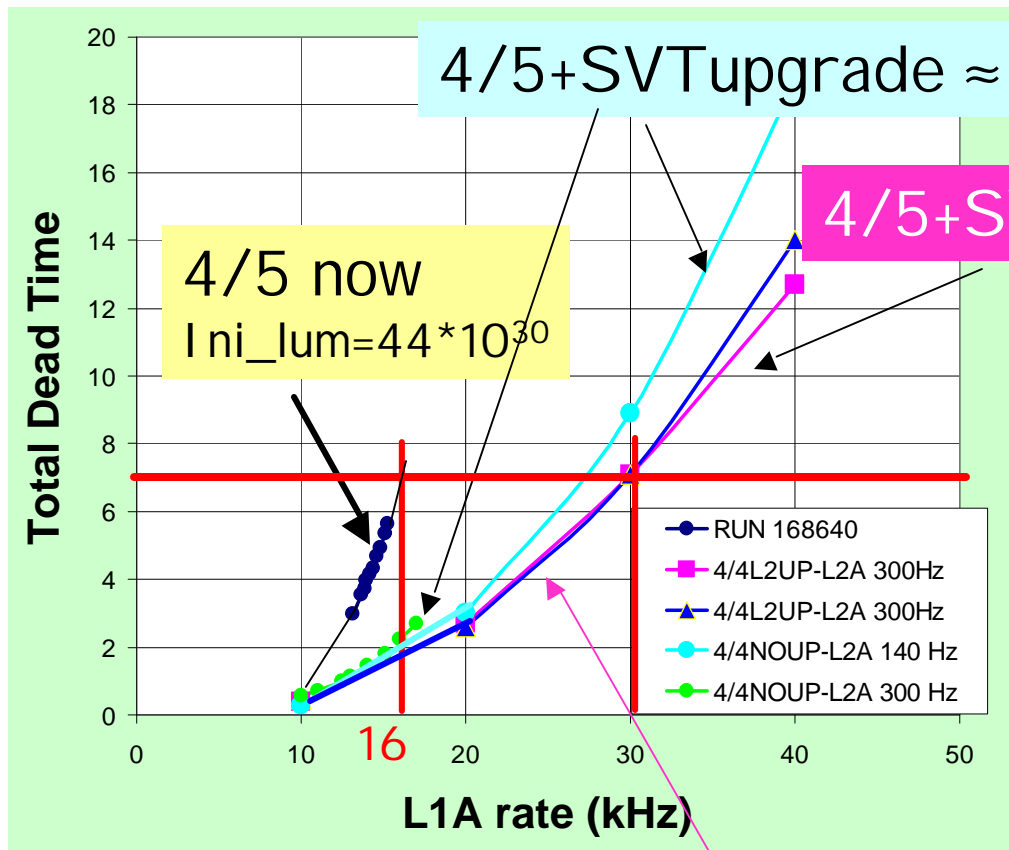
SVT is running right now @4/5



	L1_TWO_TRK_PT2 B physics	L1_TWO_TRK2_&_TWO _CJET5 Z→bb
SVTconfiguration	# of fits	# of fits
32 kpat 4/4	3.9	9.4
32 kpat 4/5 (now)	39.1	94
32 kpat 4/5 + RW	17.6	42
128 kpat 4/5 + RW	9.3	23
Ghost removal	4.3	14.5

ROAD WARRIOR + AM ++ bring us back to the old 4/4 timing, with better efficiency!

What if...



$I_{ni_lum} = 32 \cdot 10^{30}$
 $I_{ni_lum} = 17.5 \cdot 10^{30}$
 $I_{ni_lum} = 22 \cdot 10^{30}$

Forward Muons

An example of the added
flexibility

Flexibility

- The larger AM bank allows new strategies:
 1. Narrower patterns to improve timing
 2. Trigger bit dependent patterns
 3. (L1) Lepton seeded pattern recognition
 4. Standalone Si tracking
 5. ...?
- As an example we tried to merge 3. And 4. To build a forward $z \rightarrow \mu\mu$ trigger!

Forward Muons Trigger

$1 < \eta < 1.25$ (FRONT) L1:

BMU*BSU(F)*XFT11

rate 8-16Hz @ 4E31

L2: RateLimited @ 0.7 Hz

$1 < \eta < 1.25$ BSU(F)

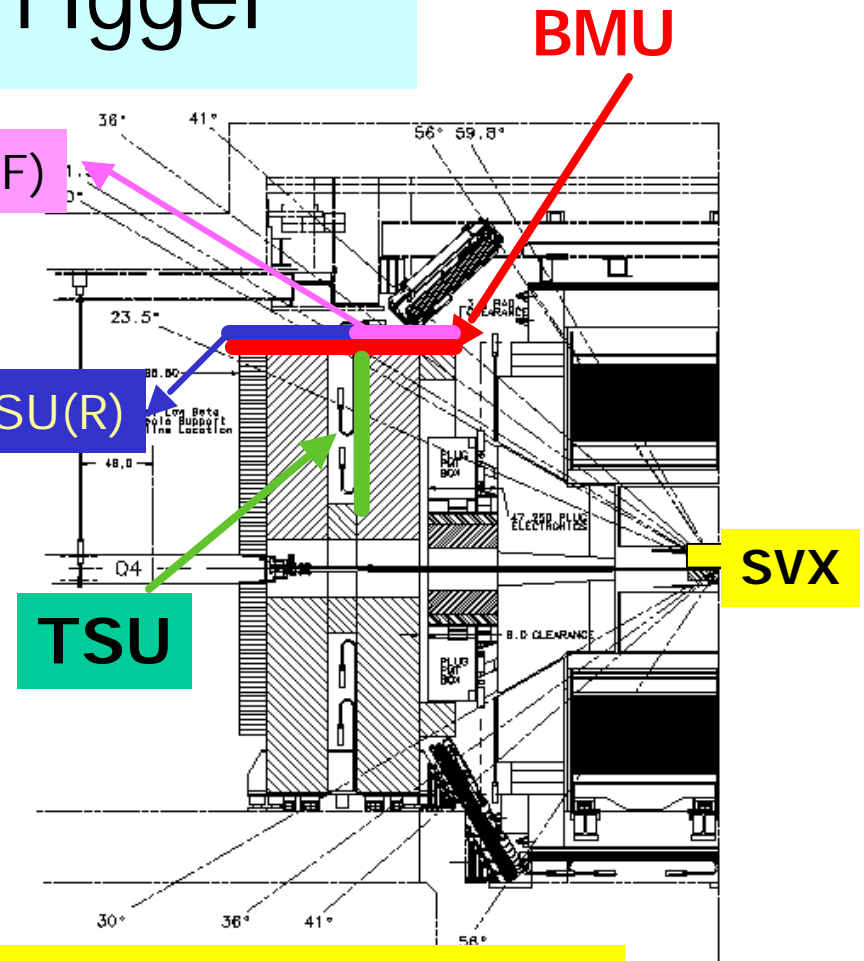
$1.25 < \eta < 1.5$ BSU(R)

$1.25 < \eta < 1.5$ (REAR) L1:

BMU*BSU(R)*TSU

Rate 200-400Hz @ 4E31

L2: RateLimited @ 1.3 Hz



We can use **SVT***BMU*BSU for a single trigger, without η bias! Goal rejection ~ 20-50.

- high Pt prompt leptons \rightarrow "only" 30kpatterns @ 95% eff.
(Pt>8 GeV [excellent down to 4 GeV] & d0<500 μ m)

In a glimpse..

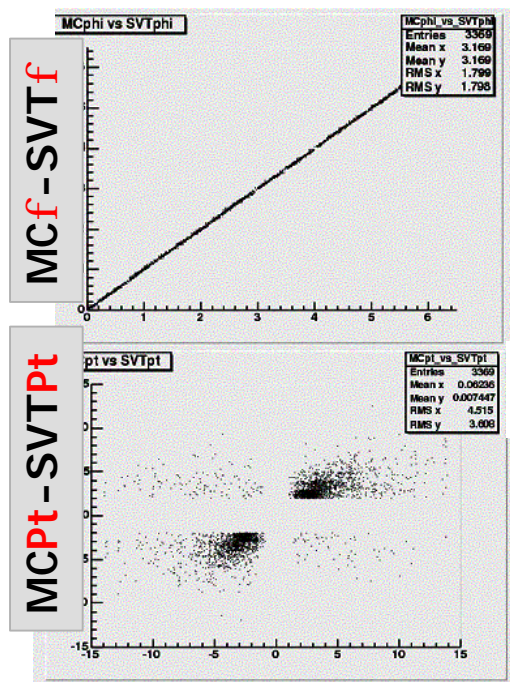
- Efficiency @ L2: study $Z0 \rightarrow \mu\mu$ from data
- Back. Rejection: L1 backup from data

Selection	# Z0	# L1_BMU_REAR
L1_MU	250	4678
match $\Delta\phi < 2.5^\circ$ Pt > 4 & $\chi^2 < 10$	132	362
+ η match	126	213
L2 Eff.	0.50	
L2 Rej.		22

Tracking Performance

This is SVT doing standalone SVX tracking **ON THE FLY!!!**

MC(J/Psi): generator vs SVT L1_MU data: offline vs SVT



$$\sigma(\phi)=0.007 \quad \sigma(\phi)=0.008$$

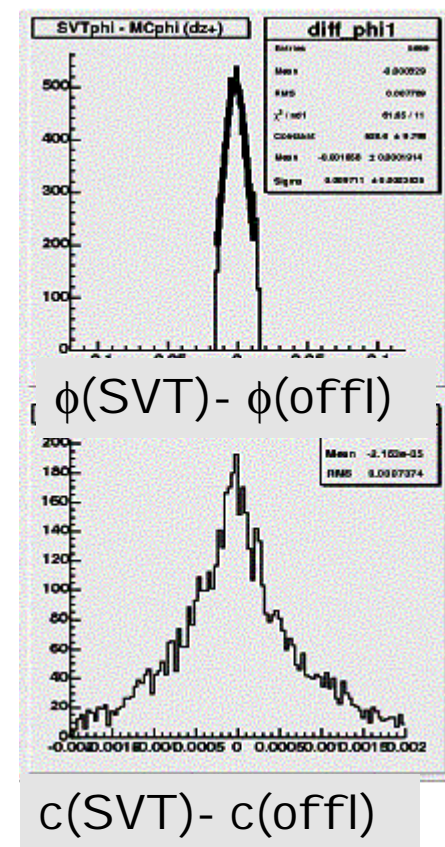
$$\sigma_{Pt/Pt^2}=0.08 \quad \sigma_{Pt/Pt^2}=0.095$$

Offline standalone Si

(from **TDR**):

$$\sigma(\phi)=0.002$$

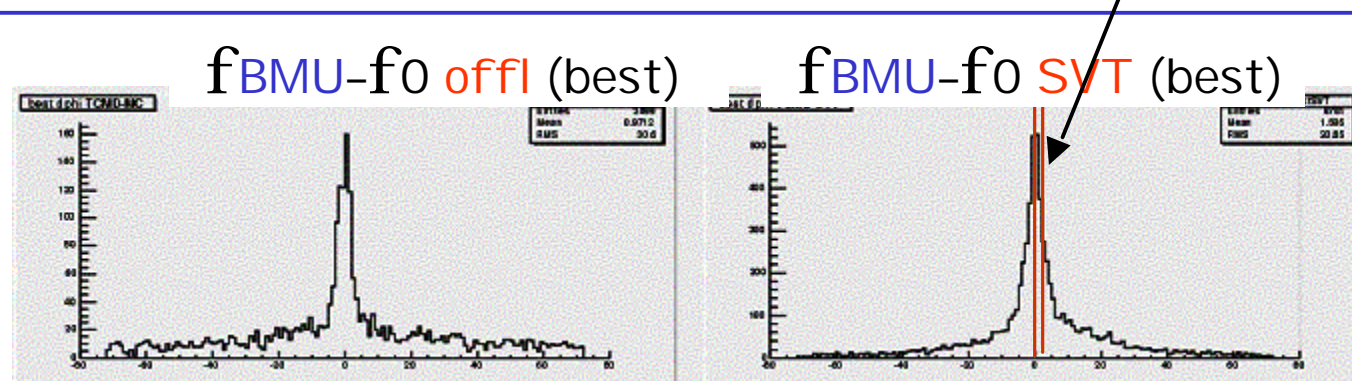
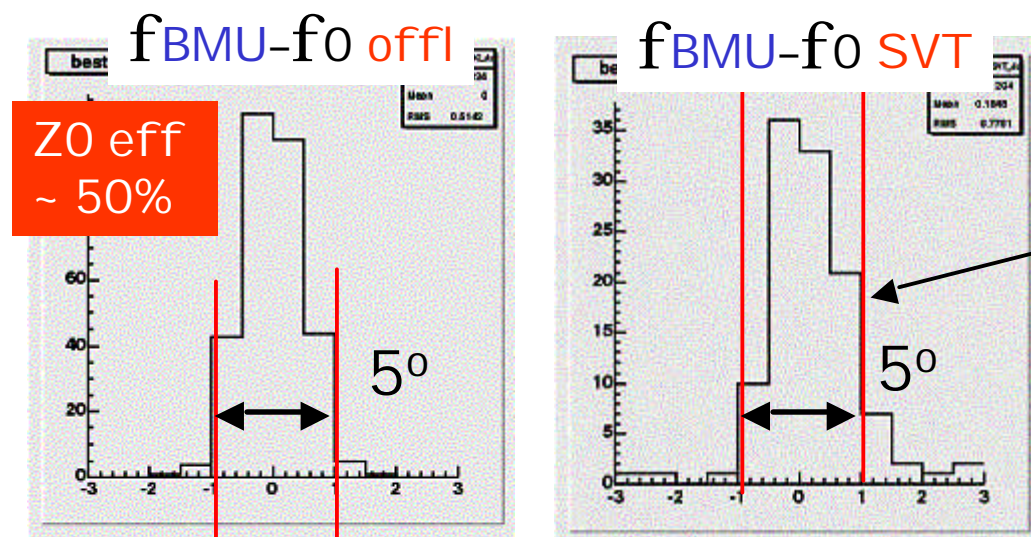
$$\sigma_{Pt/Pt^2}=0.07$$



Occupancy is huge! → seed SVT with muons!

Forward muons as SVT seeds!

Z0->mm data: $P_t > 4$ & $c^2 < 10$



Rejection from L1 MU data: ~22

New Hardware Summary

Road Warrior

- Implemented on PULSAR HW, with **no changes**
- Further reprogramming **could help SVT**:
 - Cope with ageing hardware (AMS & HB)
 - Provide new functionalities*:
(See next slide for examples!)

* Might need hardware add-ons

SVT II?

- Pulsar reprogramming leaves open the option of increasing the SVT performance “ad libitum”:
 - More flexibility in pattern handling
 - 1M pattern?
 - More than 5 layers?
 - Multiple PID sources (TOF, muons, electrons)
 - 3D tracking?
 - Pattern “segmentation”:
 - “Trigger bit awareness”: can decide how to seed pattern recognition/track fitting depending on L1 bits!
 - Potentially could even activate/deactivate some of these features based on a partial outcome of the pattern recognition stage!

AM++

- Replace old AM boards with 1 AM++/wedge
 - Increased pattern density: standard cell chips (2K [\leftrightarrow 128] pattern/5x5 mm)
 - Potentially larger I/O bandwidth
 - Provide backward compatibility with older hardware?
 - Can house potentially up to 1Mpattern!

AM++ schedule

- **New AM-board**: summer 2004 (Pisa)
during summer 2004: test with FPGA chips (Pisa)
- **AM-chip design**: july 2004 (Ferrara-Pisa)
first chip ~2 months → october
- **New LAMB**: assemble AM-chip in october 2004
(Pisa)
- **test chip + board**: october – december 2004
(Pisa-Ferrara)
- **Mass production**: beginning 2005 (Pisa-Ferrara)
- **install**: summer 2005 (Pisa-Ferrara)

Impact on data taking

- Boards can be completely developed and tested in test-stands
- Algorithm development & tuning may require some test runs
- Overall the experiment dead time will come from:
 - Boards swapping
 - Development/modification of online code
- Everything will be back-compatible: virtually no point of no-return!

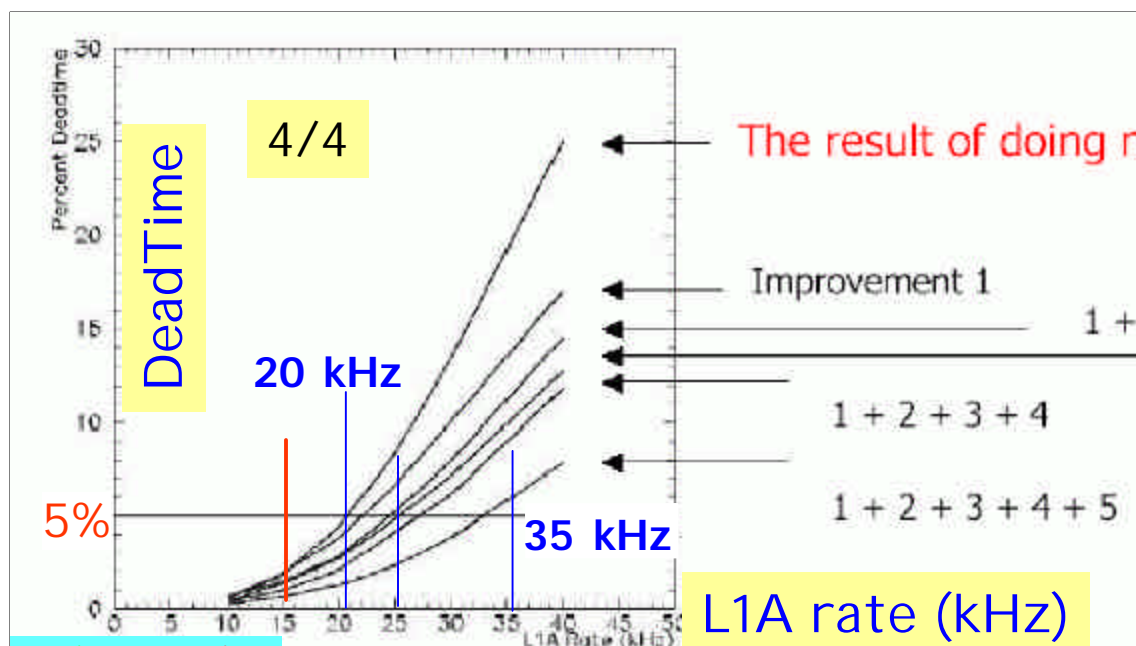
Conclusions:

- L2 Timing is critical in the CDF DAQ
- SVT is critical to the L2 Timing
- RW & AM++ helps improving SVT efficiency with reasonable timing
- Both address also the issue of ageing of critical components:
 - AMS & HB
 - AM Chips/boards
- RW is a PULSAR → Provides additional flexibility:
 - Change RW algorithms
 - Open to new SVT options

Backup

ModSim (What If...)

1. Two SRCs in parallel
2. L2 processor upgrade
3. 8®7 bit SVX digit.
4. -3 ms in SVT proc.time
5. cut SVT tails above 27 msec

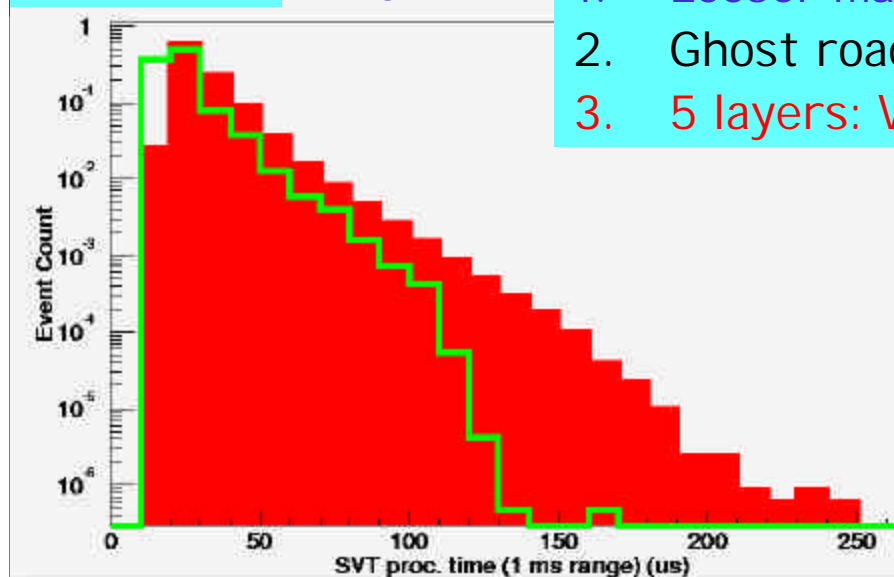


BUT the recent use of 4/5 in SVT changes the conditions!

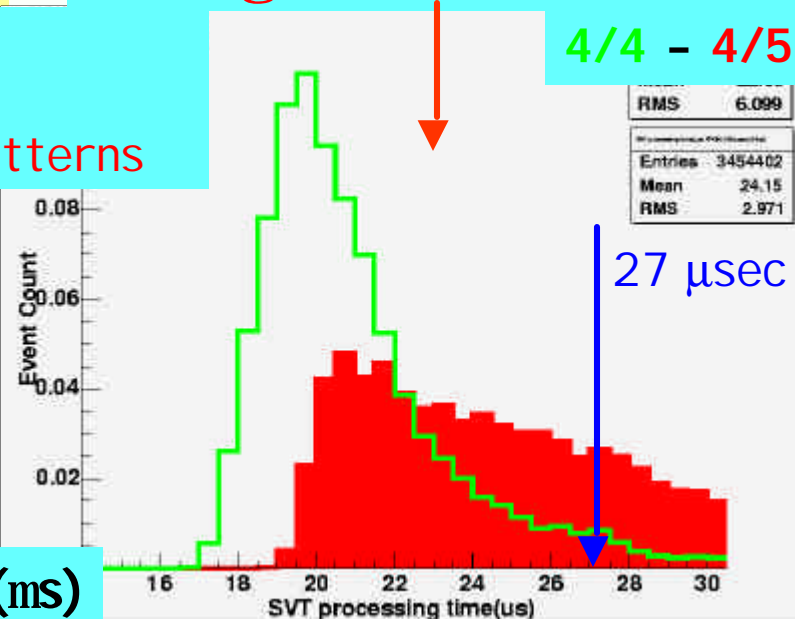
4/4 - 4/5

1. Looser match
2. Ghost roads
3. 5 layers: Wider Patterns

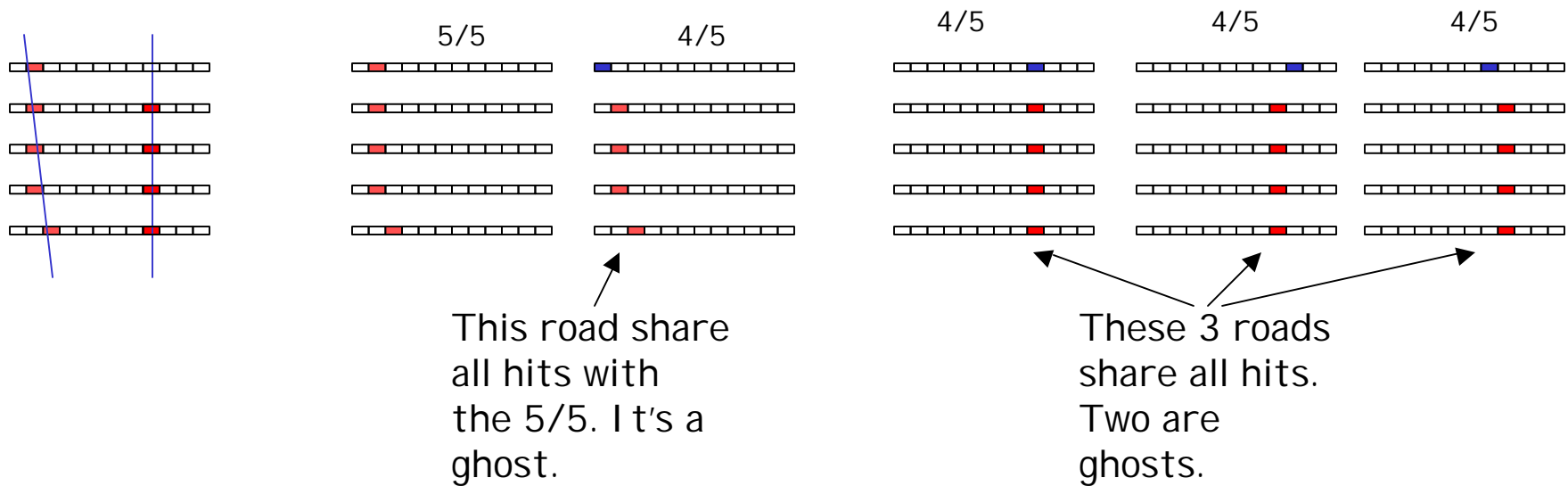
4/4 - 4/5



Time (ms)



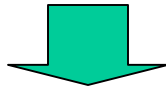
Why 4/5 is more complex?



Ghosts are 60-70% of 4/5 roads.

Removing them speeds up 4/5 processing time.

NOW pattern recognition with 5 SVX layers uses
larger patterns w.r.t. 4 SVX layers



More **fake roads** and more **hits** inside roads

Solution: More AM → thinner patterns → reduce fakes