SVX3D Chips :

Availability and Usage

Igor Volobouev

LBNL

http://cdfsg6.lbl.gov/~igv/chipcount.ps

Chips Needed

- Layer 00 : 108 chips in the detector
- SVX : 3168
- ISL : 2368
- "Barrel-4" : 242 (2 for L00, 176 for SVX, 64 for ISL)

  Total baseline chip count: 5886

Extra ladders and hybrids: +2014

Prototyping, testing: +500

Total: 8400

SVX3D Wafer Count

SVX3D wafers were produced by Honeywell SSEC in a radiation hard 0.8μm CMOS process.

- 4 in. runs (2-7): 119 wafers, 6188 chips.
- 6 in. runs (8-16): 102 wafers, 13788 chips. Wafers returned to Honeywell are not counted.

19976 chips looks like a large number. However, it becomes much smaller when all the yields are factored in:

- Wafer yield
- Backgrinding and backplating
- Dicing and picking
- Hybrid assembly
- Ladder assembly
- Handling (mechanical damage, ESD, etc.)

SVX3D Wafer Probing

All SVX3D wafers have been probed. The set of tests included various functionality checks (pipeline logic, ADC, readout, etc.) as well as measurements of pedestals, gain, and noise.

Chip classification

- GOOD: passed all tests
- FAIR: not more than one channel and/or 30 pipeline capacitors are bad
- BAD: all other

Due to various manufacturing defects, chips from the 6 in. Honeywell line had much higher failure rates than the 4 in. chips. See TM-2081 report by Ray Yarema for details.

SVX3D Wafer Yields

4 in. Honeywell runs

Dice probed:	6114	(100 %)
Good dice:	3091	(50.6 %)
Fair dice:	708	(11.6 %)

6 in. Honeywell runs (not including returned wafers)

Dice probed:	13788	(100 %)
Good dice:	4845	(35.1 %)
Fair dice:	2024	(14.7 %)

Total number of good and fair dice available after wafer probing: 10668

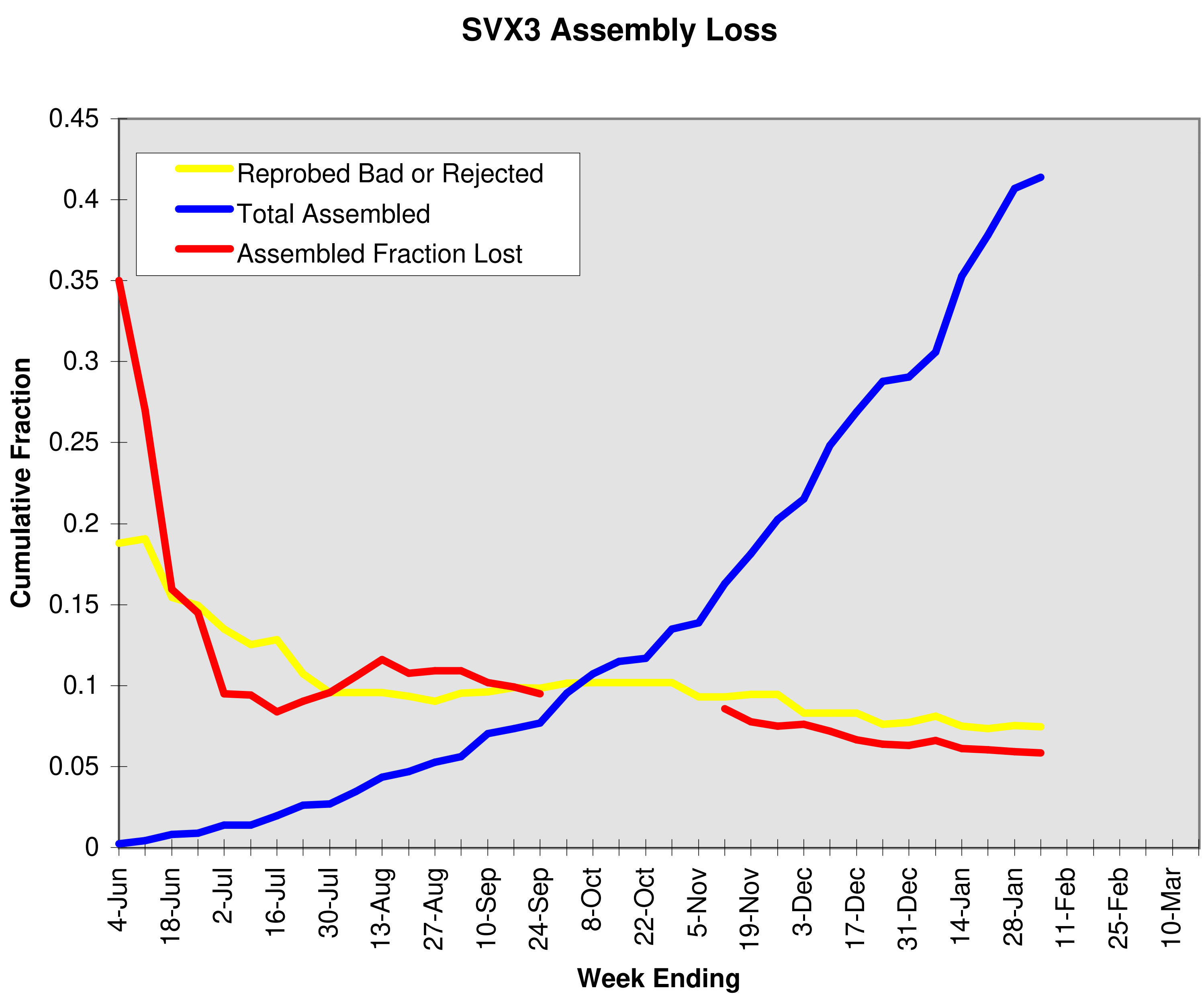
The wafer quality maps are on WWW at
http://cdfsg6.lbl.gov/~igv/svxmaps.html

Other Yields

- Backgrinding and backplating: no yield loss observed for dice on wafers, but one 4 in. wafer was broken.
- Dicing (and, perhaps, picking): chip failure rate is about 10% for 4 in. wafers and 2% for 6 in. wafers. There is no obvious pattern in the types of failures. Also, 2% of the chips are rejected at AMA during visual inspection.
- Hybrid assembly: about 6% of chips are replaced, or junked together with bad hybrids.

  The number of available chips is reduced to 9300

- Ladder assembly: yield is already taken into account by virtue of the "extra ladders and hybrids" category.
- Handling: an inherent part of all the losses above.


SVX3 Assembly Loss
Reprobed Bad or Rejected
Total Assembled
Assembled Fraction Lost
Cumulative Fraction
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
4-Jun
18-Jun
2-Jul
16-Jul
30-Jul
13-Aug
27-Aug
10-Sep
24-Sep
8-Oct
22-Oct
5-Nov
19-Nov
3-Dec
17-Dec
31-Dec
14-Jan
28-Jan
11-Feb
25-Feb
10-Mar
Week Ending

http://cdfsg6.lbl.gov/~ykkim/svx/index_chip.html

SVX3 Chip Inventory (Feb. 8, 2000)

Usage of Chips

Detector	Total	Used	Needed
L0-p	130 x 2 = 260	107 x 2 = 214	46
L0-z	130 x 2 = 260	107 x 2 = 214	46
L1-p	120 x 3 = 360	91 x 3 = 273	87
L1-z	120 x 3 = 360	99 x 3 = 297	63
L2-p	110 x 5 = 550	74 x 5 = 370	180
L2-z	110 x 5 = 550	76 x 5 = 380	170
L3-p	110 x 6 = 660	72 x 6 = 432	228
L3-z	110 x 4 = 440	71 x 4 = 284	156
L4-p	110 x 7 = 770	45 x 7 = 315	455
L4-z	110 x 7 = 770	48 x 7 = 336	434
ISL	340 x 8 = 2720	250 x 8 = 2000	720
L00	200	9	191
Total	**7900**	**5124**	**2776**

Chip Count Summary

- All available SVX3D wafers have been probed. Average yield of good dice on these wafers is 40%, yield of good+fair dice is 54%.
- Taking into account yield losses in all wafer processing and hybrid assembly steps, we have 9300 SVX3D chips. This is enough to cover our need of 8400 chips and even to create a buffer which could be used in case of emergencies or screw-ups.
- The chips are used as needed by the hybrid assembly process. The rate of die reprobing is adequate for the hybrid production needs.